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Telstra DT ERPII

BTX (Version:A00)

CPU: Intel Conroe, Core 2 Duo processors in LGA775 Package.

System Chipset:

North Bridge ... Eaglelake-Q45
South Bridge ... ICH10DO

Main Memory:

Dual Channel / DDR-III * 4 (Maximum to 8GB)

On Board Device:

Clock Generator ... SILEGO_SLG8XP523TTR
Super I/O ... SMSC5544
LAN ... BCM5761 / 57780
HDA Codec ... REALTEK ALC269Q-GR/VB3
BIOS ... SPI Flash ROM-16M bit

Expansion Slots:

PCIe X16 SLOT *1
PCIe X1 SLOT * 3 ----- (PCIe SLOT *1
For Riser *1
For Wireless *1)
PCI SLOT * 2

PWM Controller:

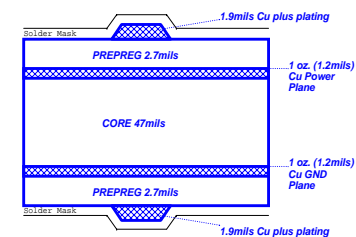
Controller ... NCP5392T (4Phase)
Driver ... NCP5359AMNR2G

POP1	Proto Build	XDP, LPC HDR, SPI Debug, EEPROM
POP2	DT	SLOT2 WITH Riser SLOT3 , SLOT4 , SLOT5
POP3	SFF	SLOT2 W/O Riser
POP4	ALC269Q - rev.A	
POP5	ALC269Q - rev.B	

Schematic Created By	EE:Ryan Juang DC-DC:Kasper Sun
Schematic Approved By	EE:Caven Kuo DC-DC:Andy Su

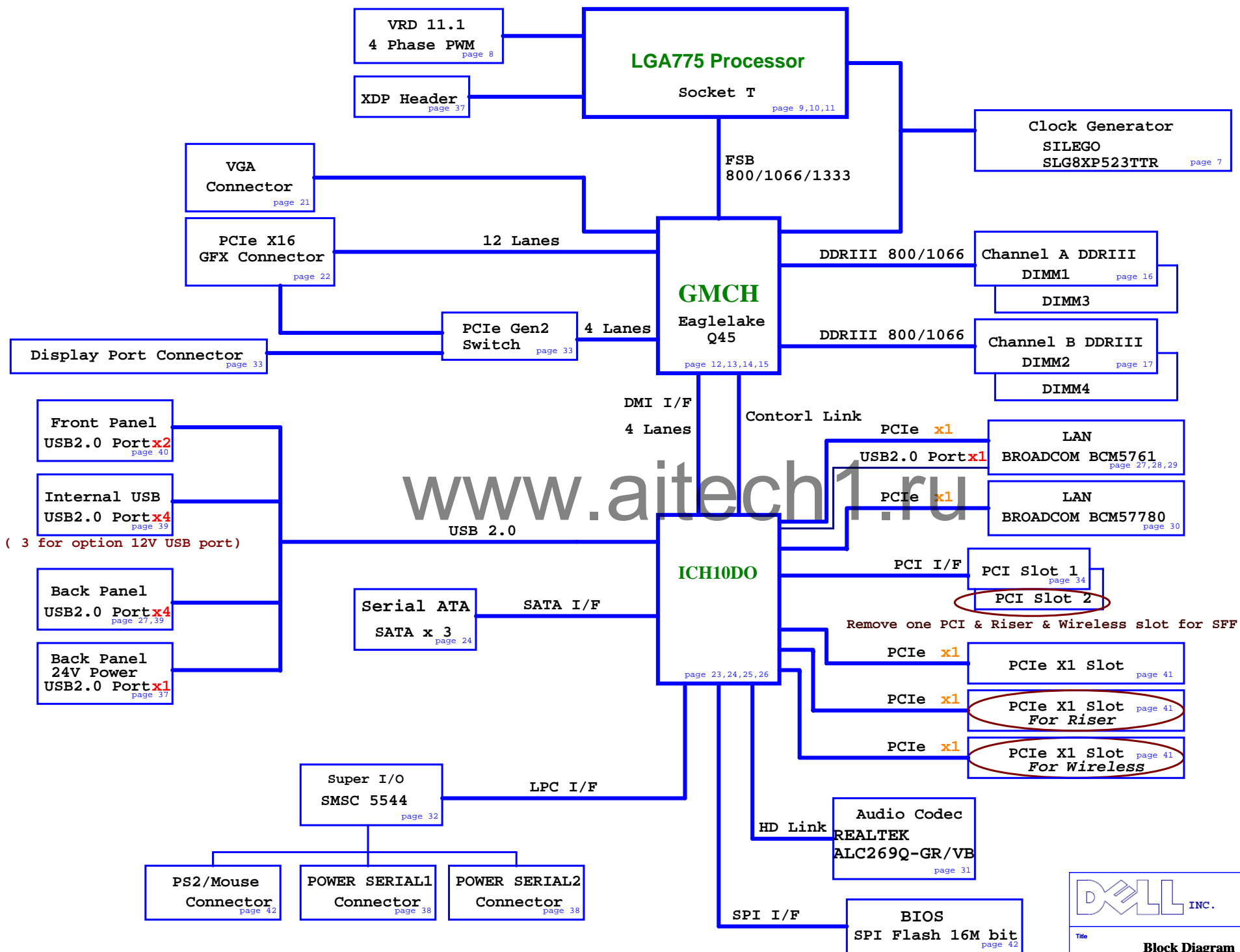
Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
PCIe - 85ohm : 15/4/8/4/15
DMI - 95ohm : 15/4/8/4/15
LAN - 95ohm : 15/4/8/4/15

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14.318MHz

CPU

CPU 200/266/333 MHz Diff Pair

MCH 200/266/333 MHz Diff Pair

PCI Express 100 MHz Diff Pair

PCIe x16 Gfx

DOT 96 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

USB/SIO 48 MHz

ICH 33 MHz

REF 14 MHz

CK PCI STOP

CK CPU STOP

PCI 33 MHz

PCI Slot 1

PCI 33 MHz

PCI Slot 2

PCI Express 100 Mhz Diff Pair

SATA 100 Mhz Diff Pair

SIO 33 MHz

PCI Express 100 Mhz Diff Pair

PCI Express 100 Mhz Diff Pair

PCI Express 100 Mhz Diff Pair X 2

XDP 100MHz Diff Pair / PCI Express 100 Mhz Diff Pair

GMCH
Eaglelake

DDRIII 4 Slots 8 Diff CLKs

Channel A DDRIII

DDRIII 800/1066

DIMM1

DIMM3

Channel B DDRIII

DDRIII 800/1066

DIMM2

DIMM4

ICH10

32.768KHz

Azalia Bit Clock

SUSCLK

Super I/O

HD Audio

BCM5761

25MHz

BCM57780

25MHz

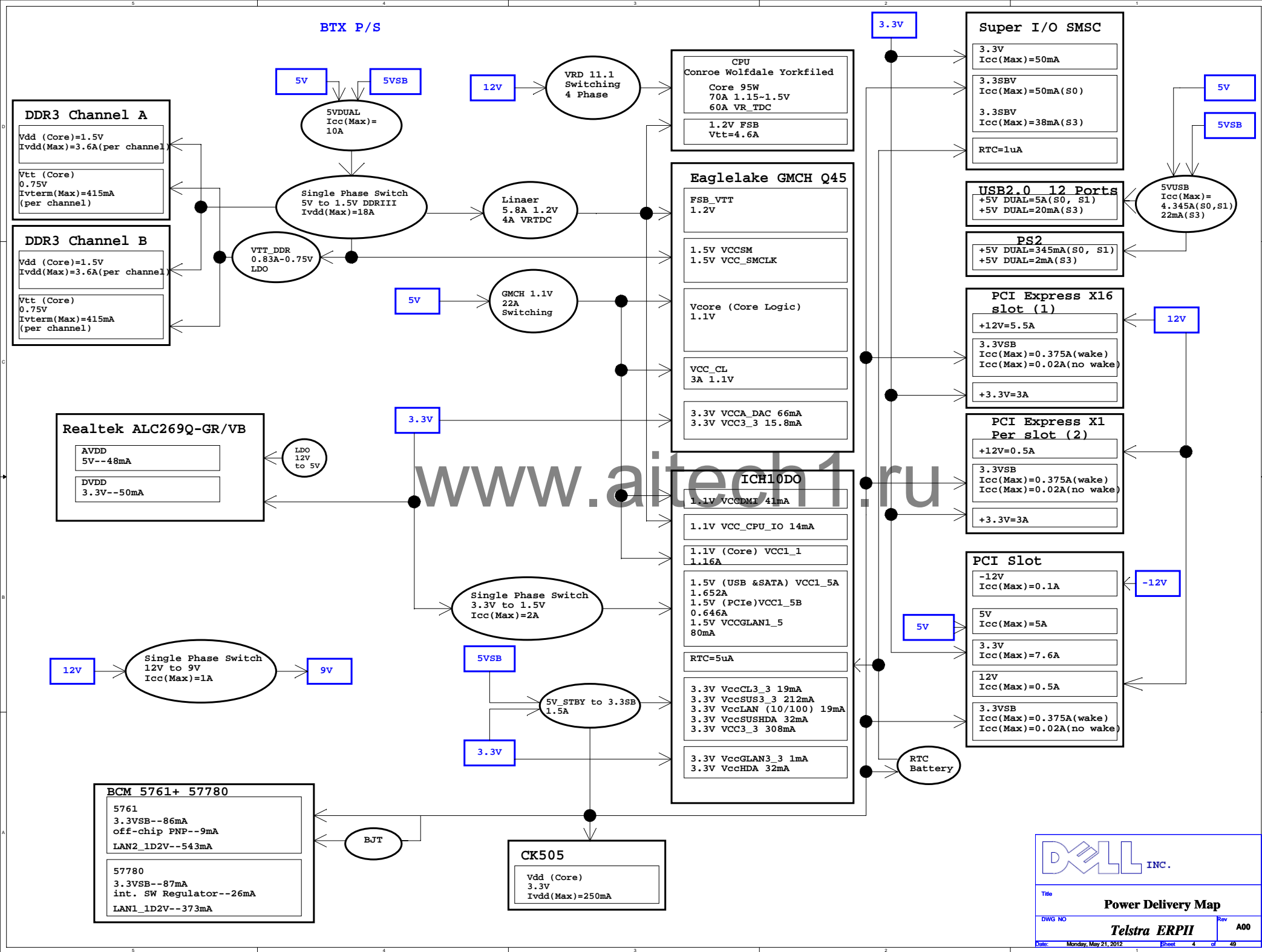
Riser / Wireless Slot

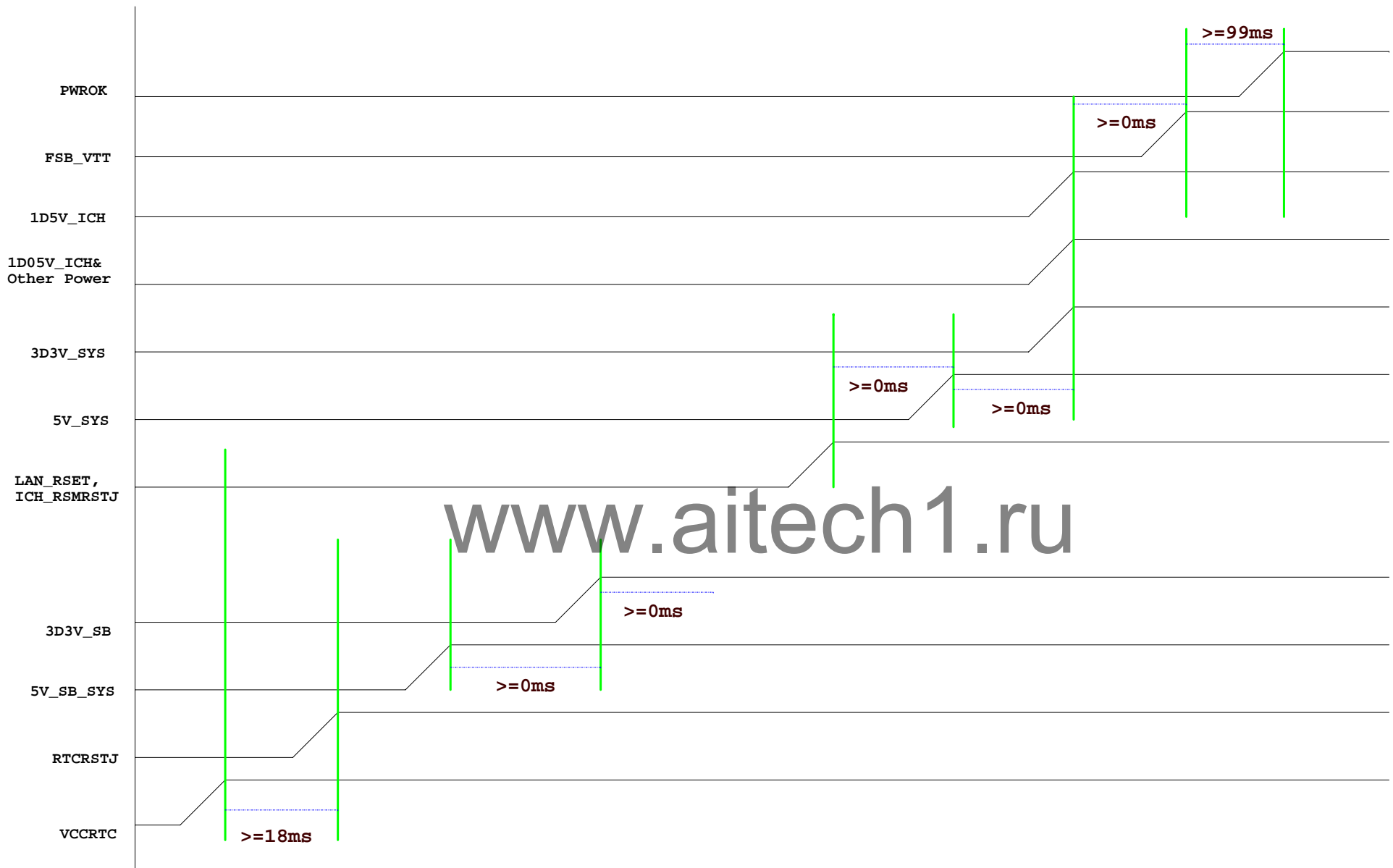
PCIe x1 Slot

XDP

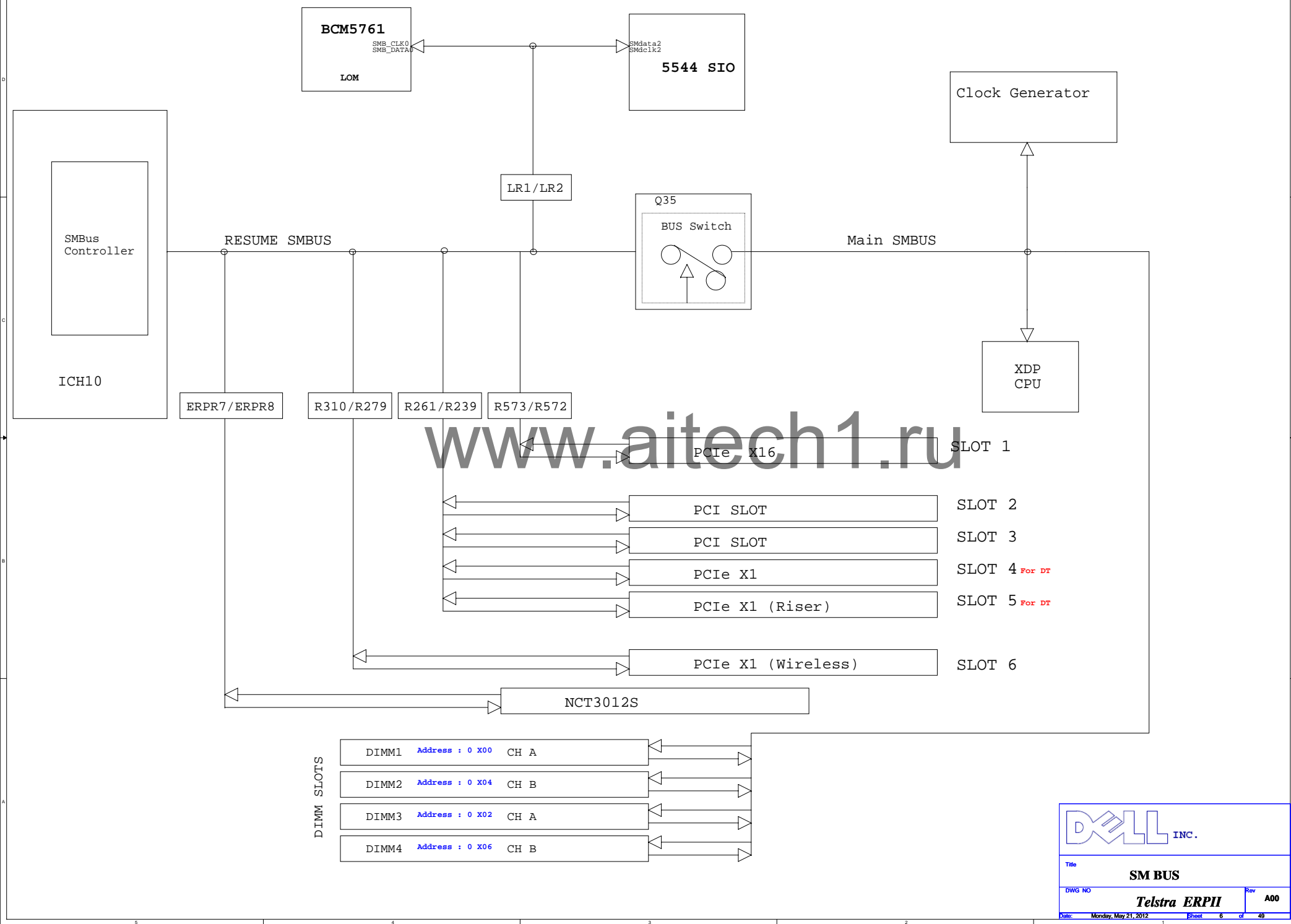
SLG8XP523TTR ClockGen

 INC.	
Title	
Clock Distribution	
DWG NO	Rev
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A00	
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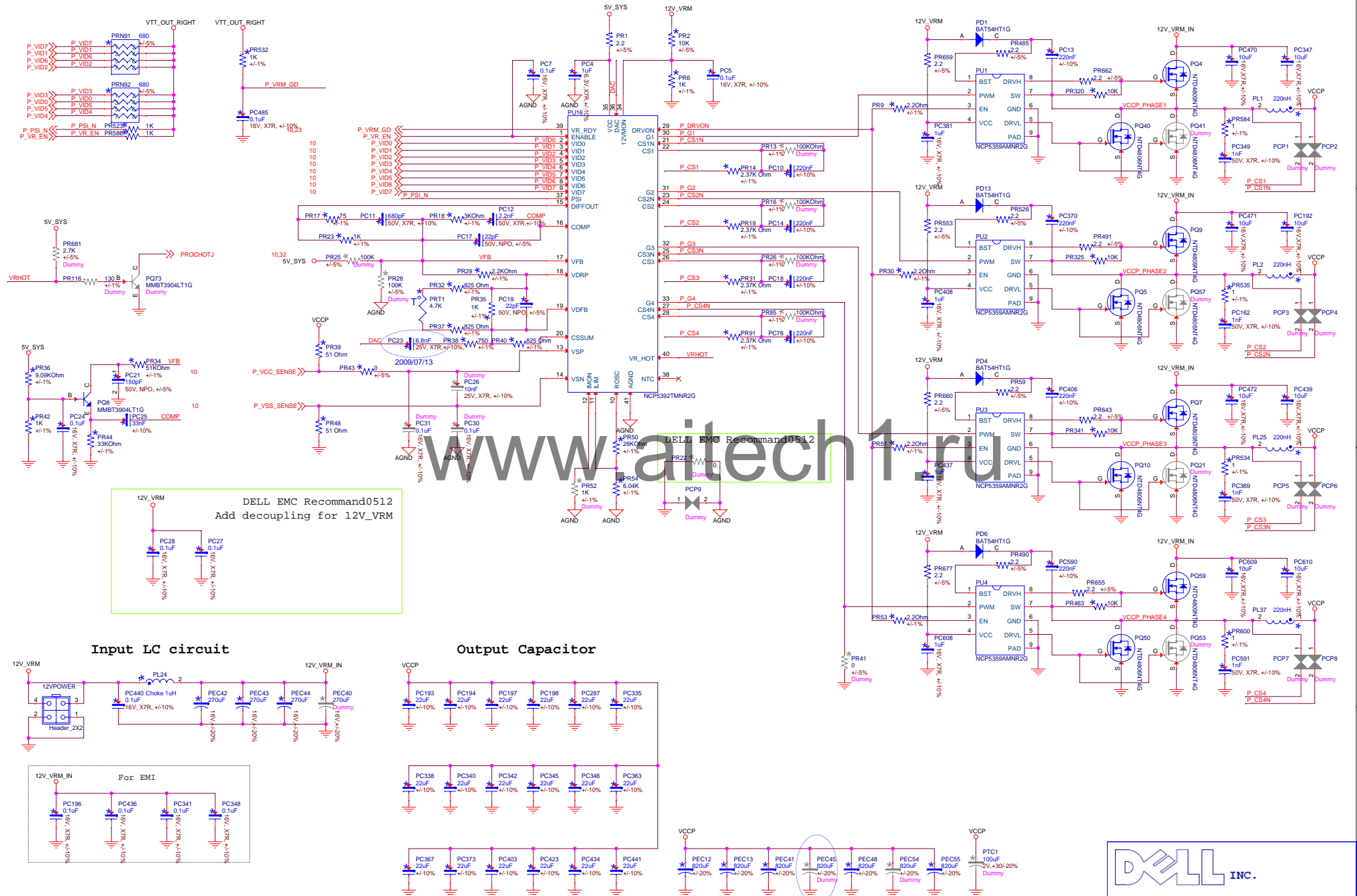


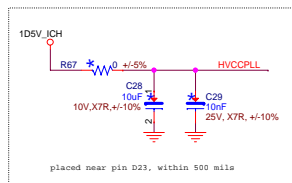
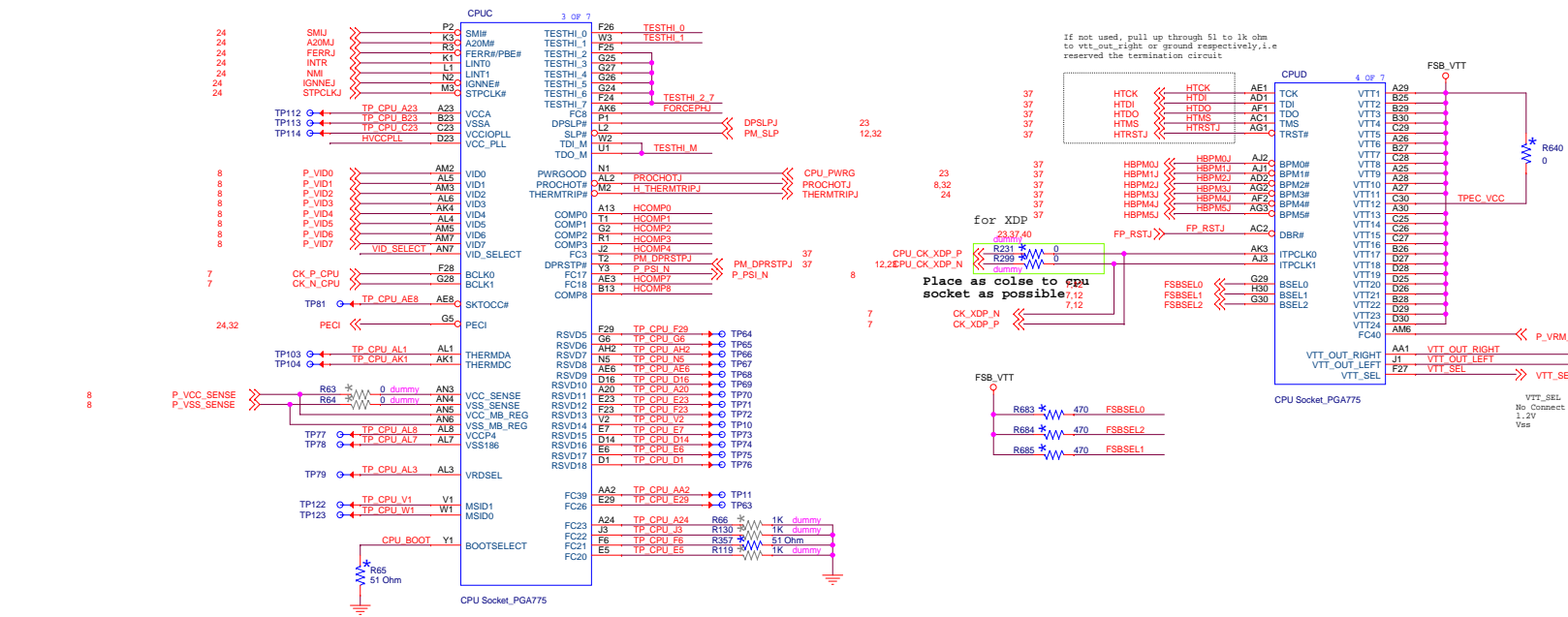


SMBUS DIAGRAM

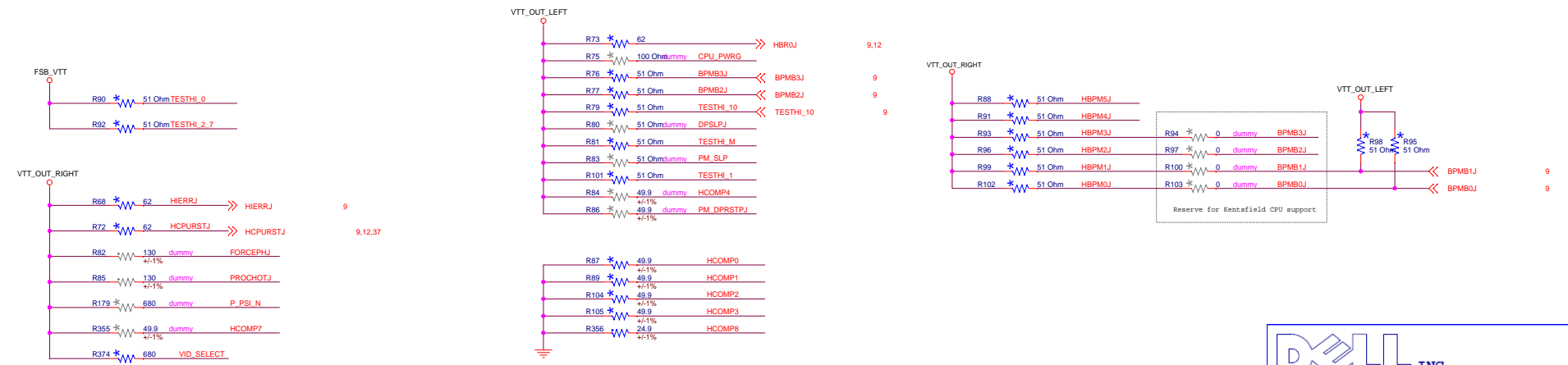


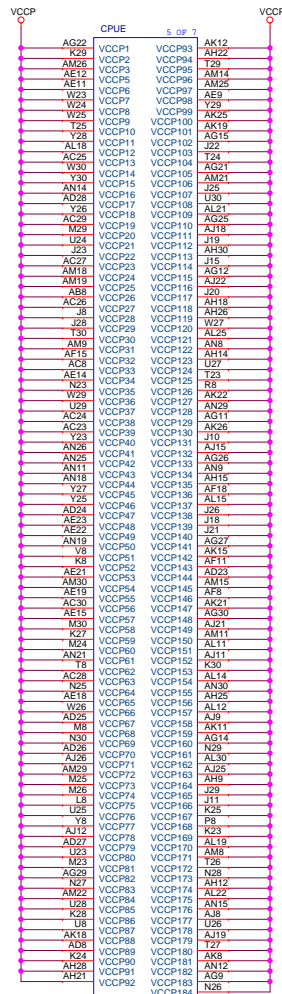
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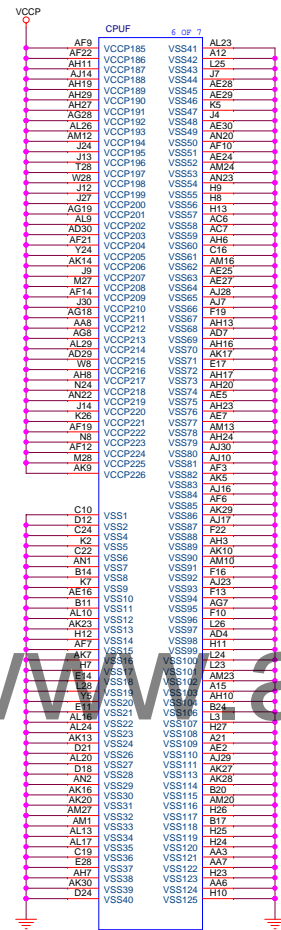


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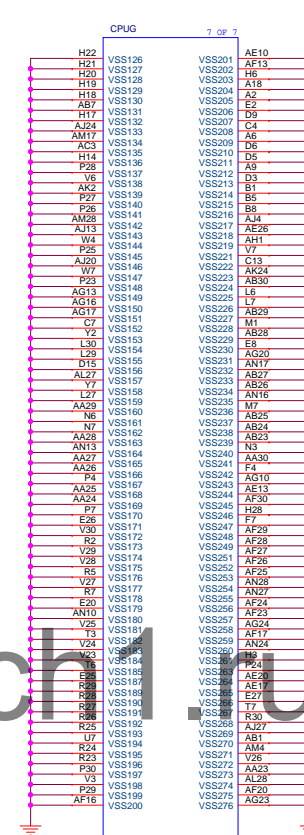




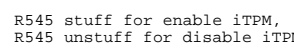
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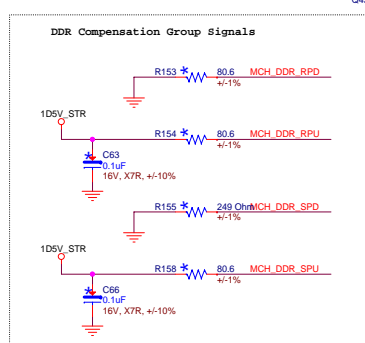
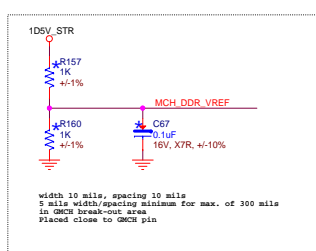
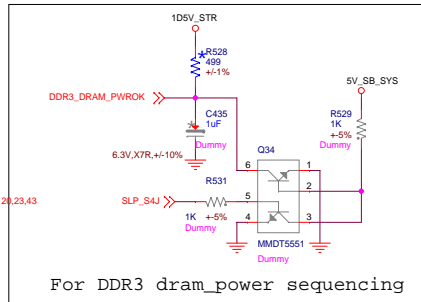
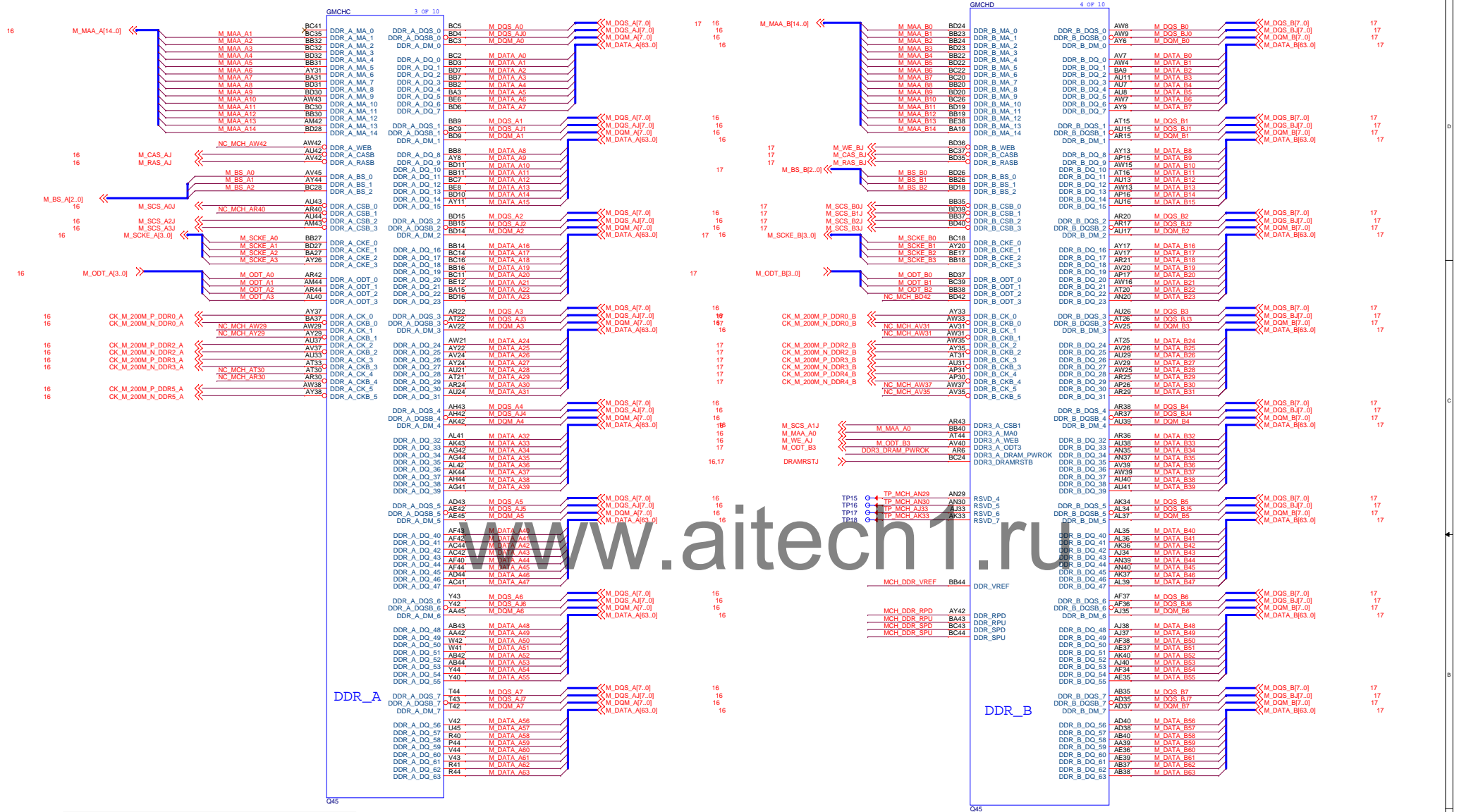


CPU Socket_PGA775



CPU Socket_PGA775



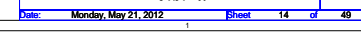
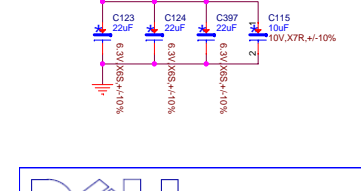
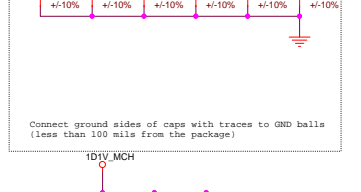
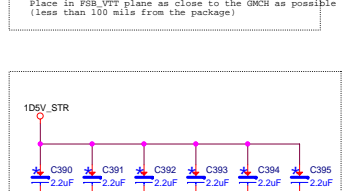
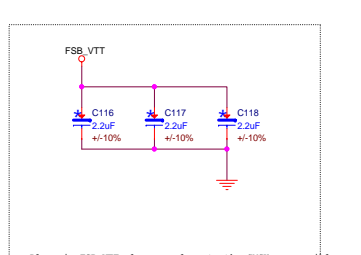
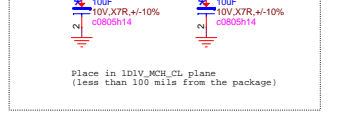
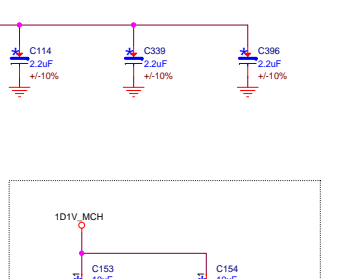
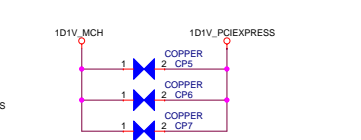
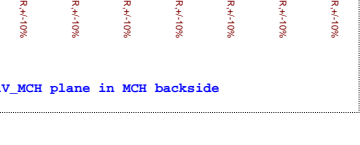
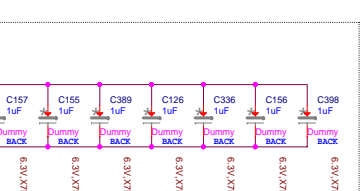
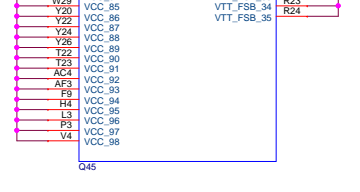
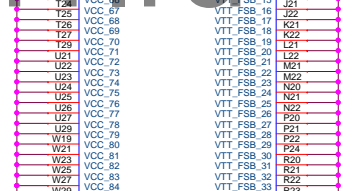
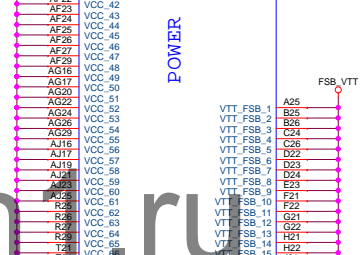
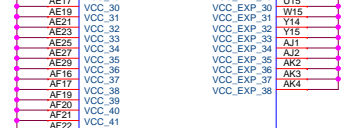
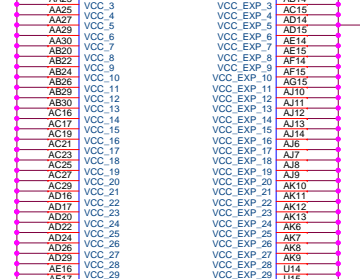
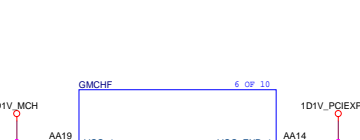
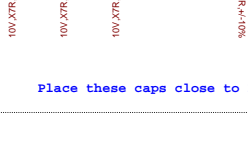
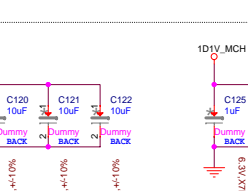
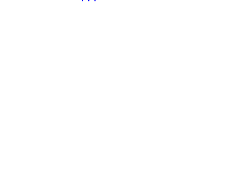
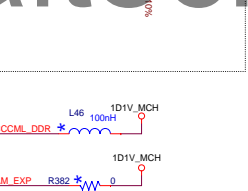
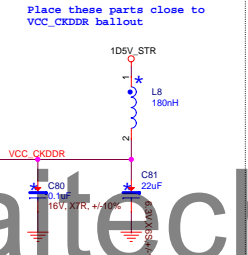
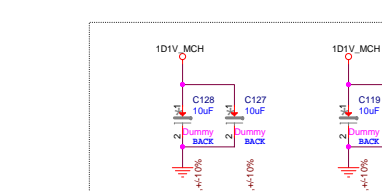
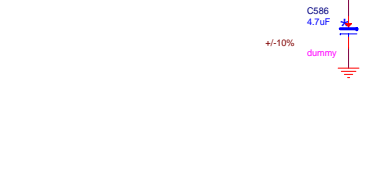
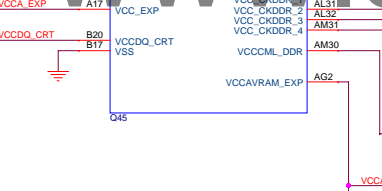
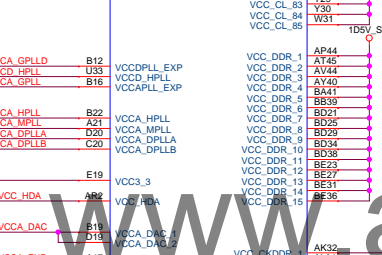
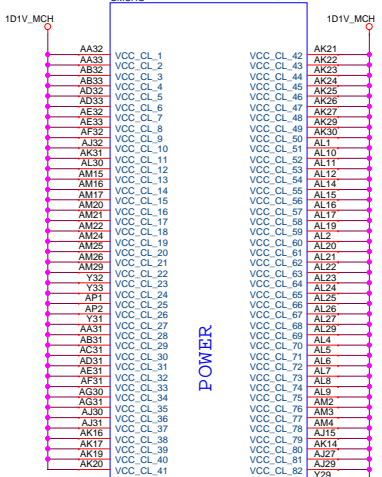
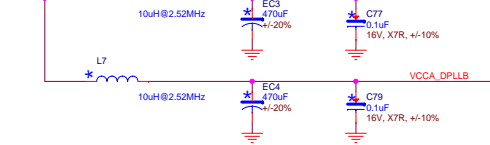
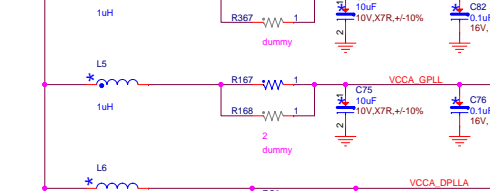
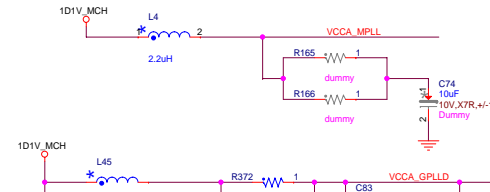
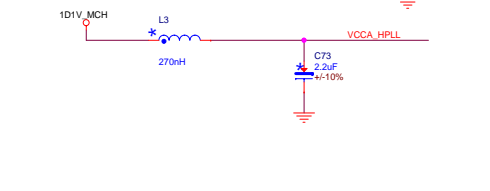
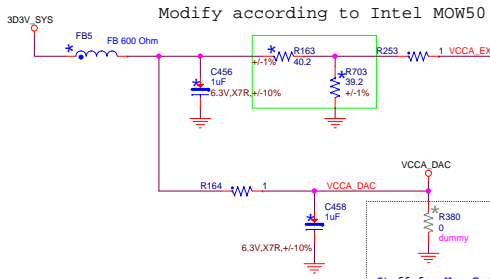
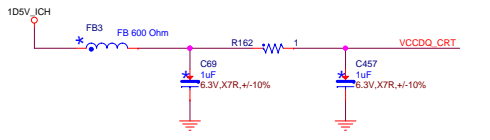


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Eaglelake -GMCH -2

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INC.

Title

Eaglelake -GMCH -3

DWG NO

Telstra ERPH

Rev

A00

Date

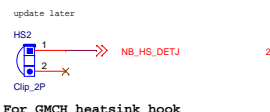
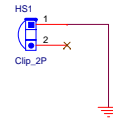
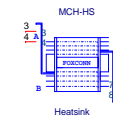
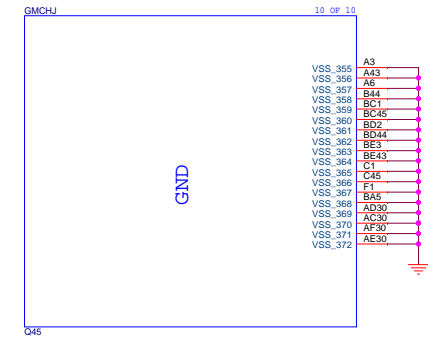
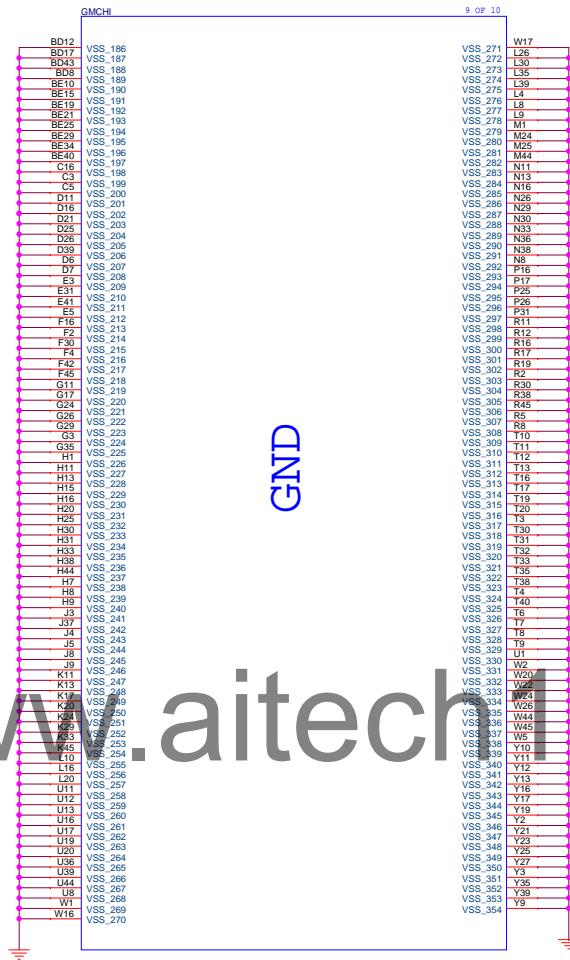
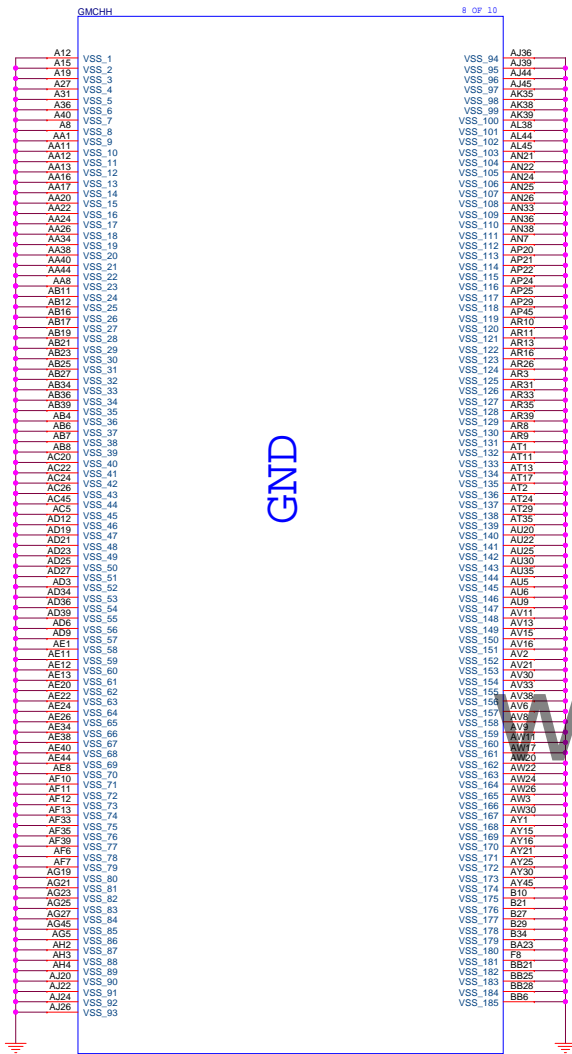
Monday, May 21, 2012

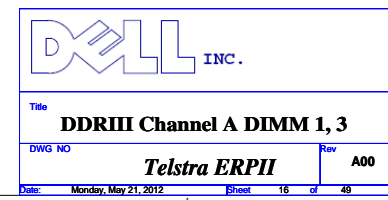
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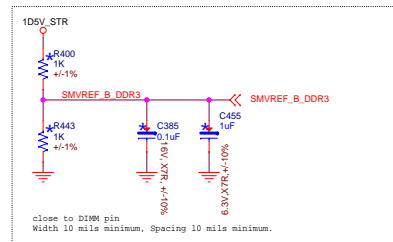
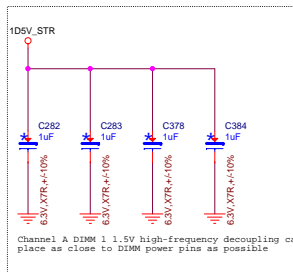
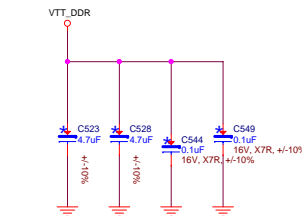
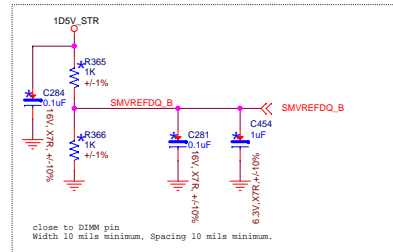
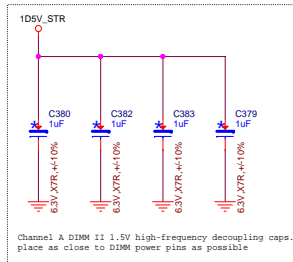
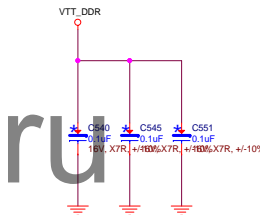
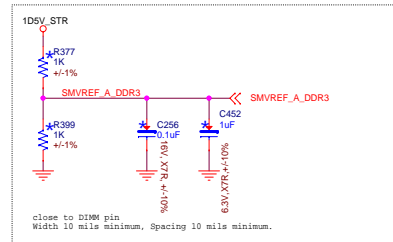
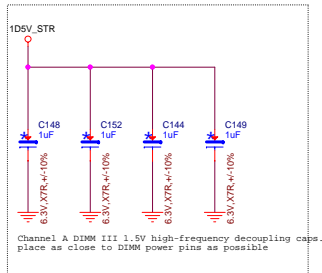
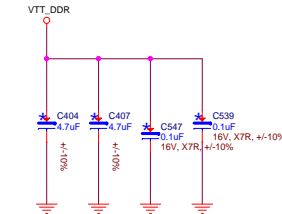
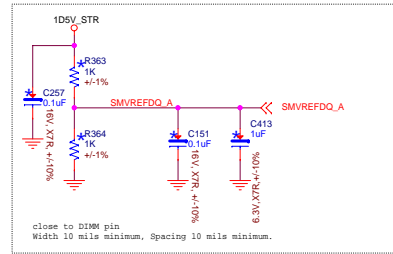
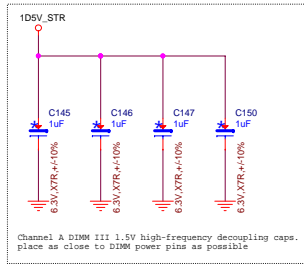
49





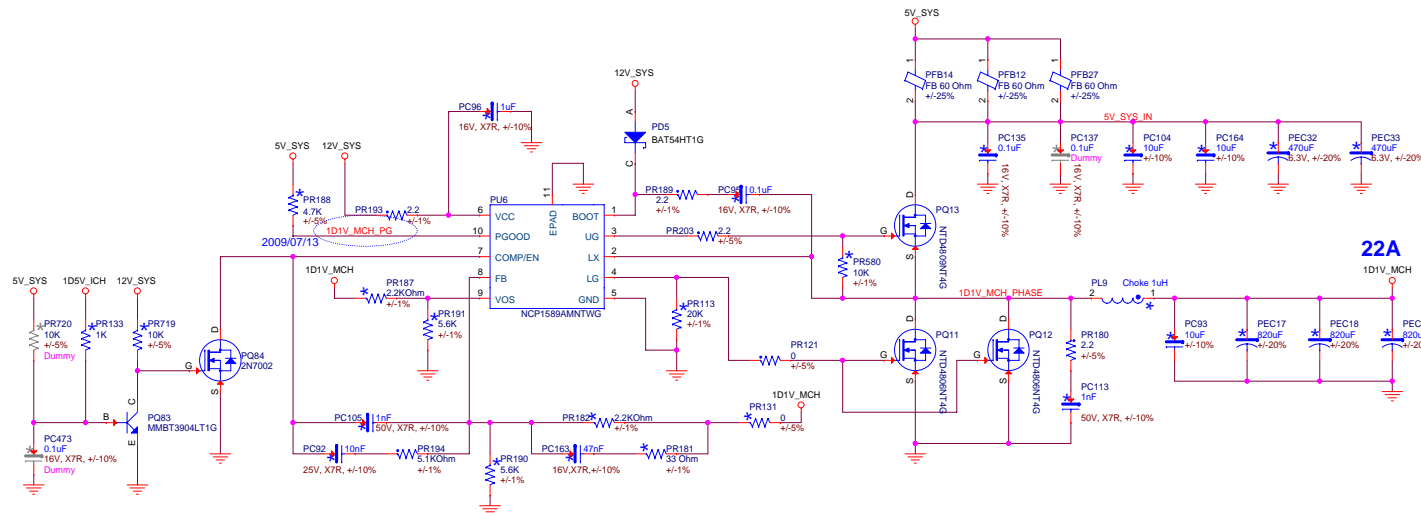


Telstra ERM II



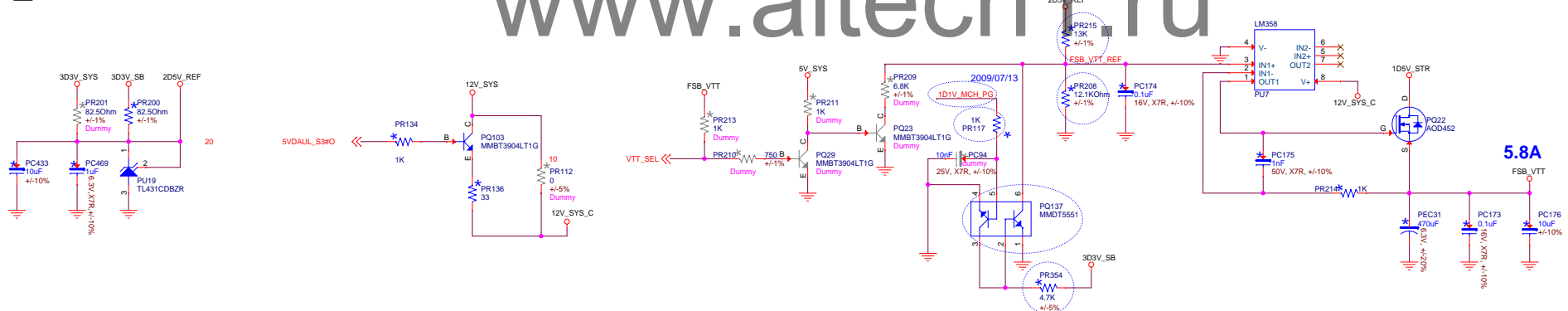
Channel B VTT_0.9V Mid Range decoupling caps.
Placed in termination Island

1D1V_MCH

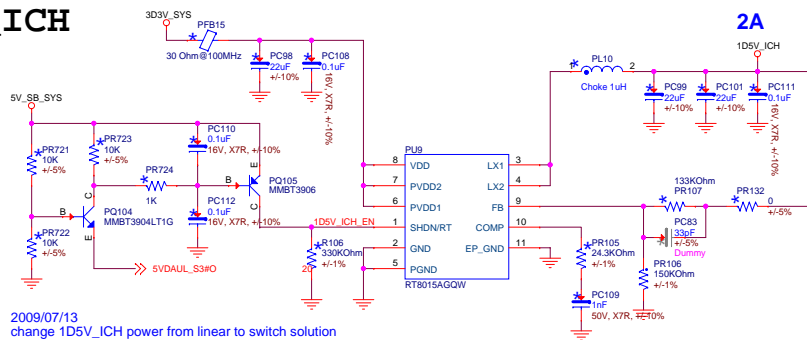


FSB_VTT

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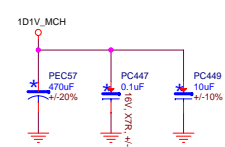


1D5V_ICH



1D1V_ICH

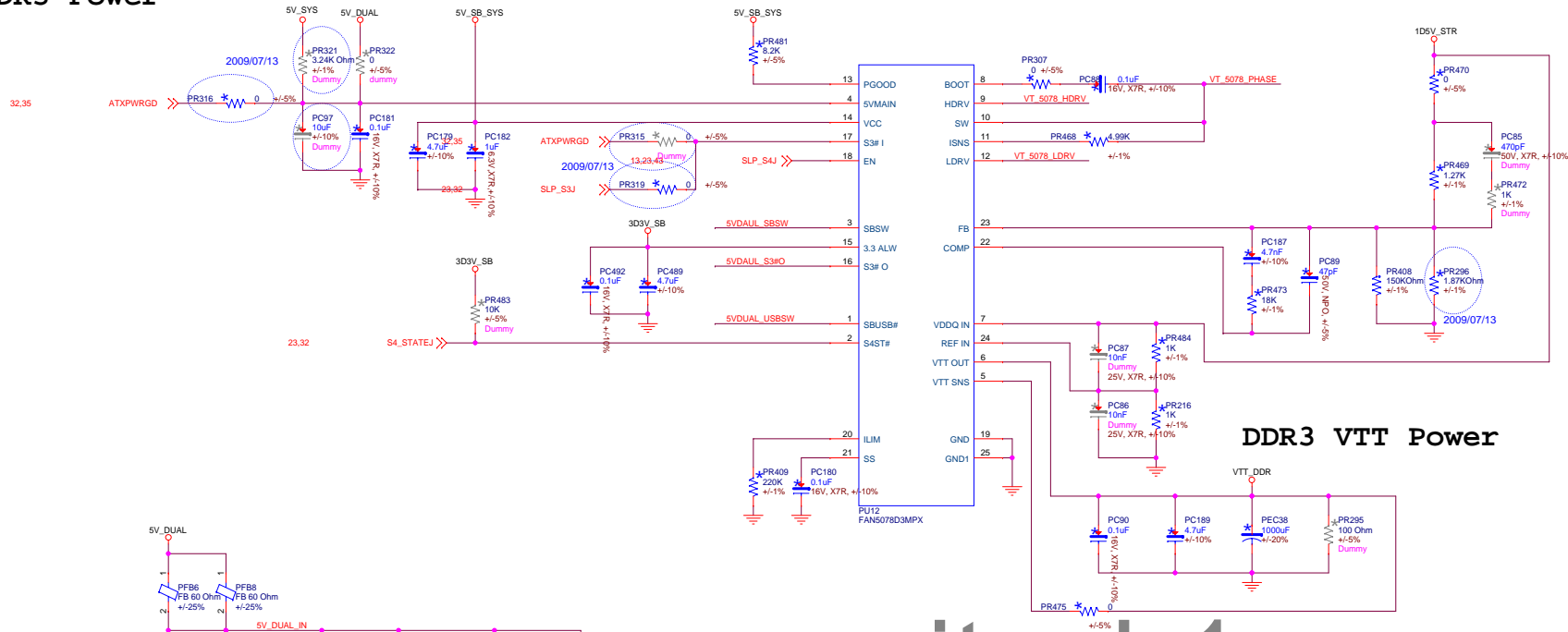
1A



Place capacitors close to Vcc1_05 in ICH

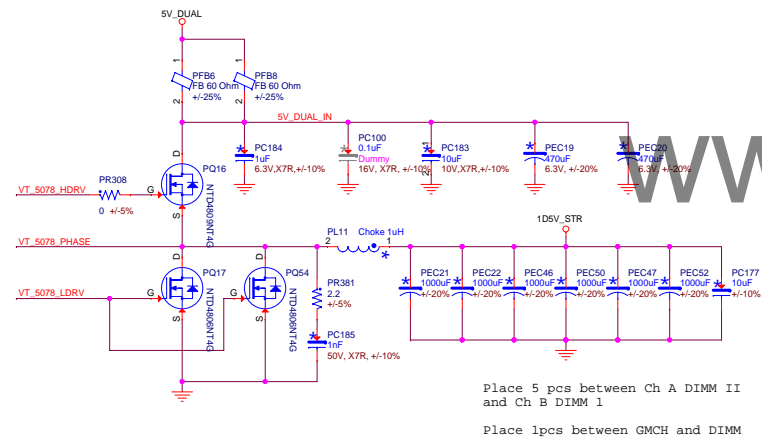
DELL INC.	
Title 1D1V/FSB_VTT/1D5V	
DWG NO Telstra ERPII	Rev A00
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DDR3 Power



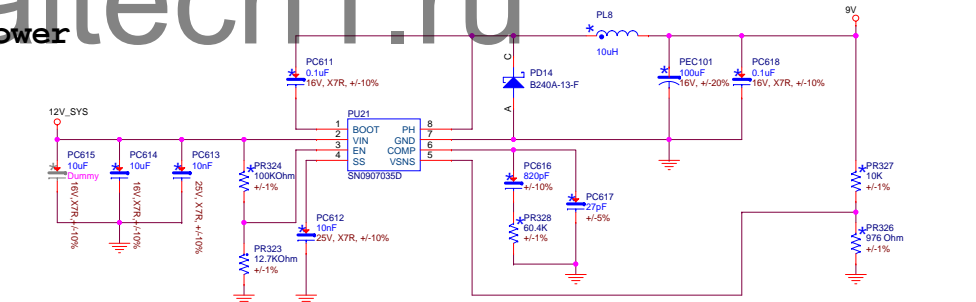
DDR3 VTT Power

9V Power

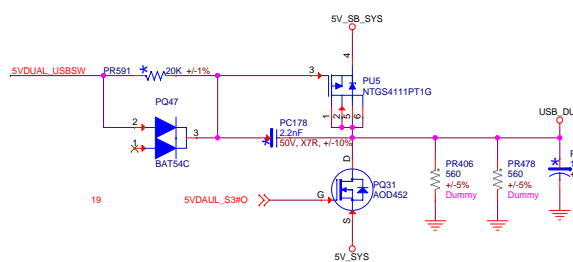


Place 5 pcs between Ch A DIMM II
and Ch B DIMM 1

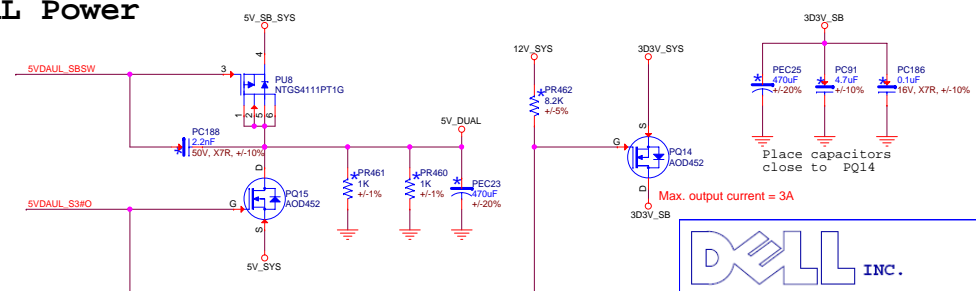
Place 1pcs between GMCH and DIMM



5VDUAL_USB_Power



5VDUAL Power

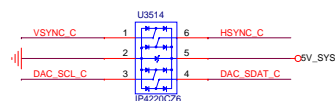
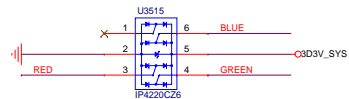
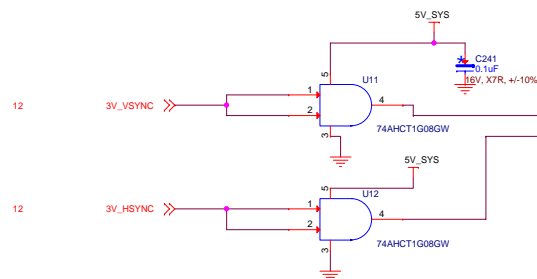


DHL INC.

Title		
STR1D5V/3D3_DUAL/5V_DUAL		
DWG NO	<i>Telstra ERPII</i>	Rev A00
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ROB TOLLING

1. from the first 150 ohm resistor to the first 150 ohm resistor: 7.5 mils(min. 6 mils spacing)
2. from the first 150 ohm res. to the second 150 ohm resistor: 4 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R,G,B should be length matched to 700 mils, max. length is 8400 mils
6. R,G,B signals should be ground referenced



The schematic diagram illustrates the board's internal components and their connections. It features three main power planes: RED, GREEN, and BLUE. Each plane is populated with decoupling capacitors (C248, C251, C249, C253, C250, C247) and resistors (R511, R510, R540, R538, R541, R539, R514, R506). The components are connected to various connectors, including L13, L14, L15, VGA, and CONN - D-SUB. The diagram also shows the connection of the 5V_SYS and 5V_GND pins to the board's power distribution network.

follow Intel MOW51

3D3V_SYS

follow Intel MOW51

R1343
8.2K
+/-5%

X16_B4

R1344
8.2K
+/-5%

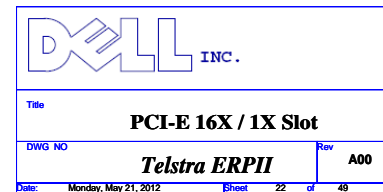
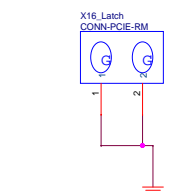
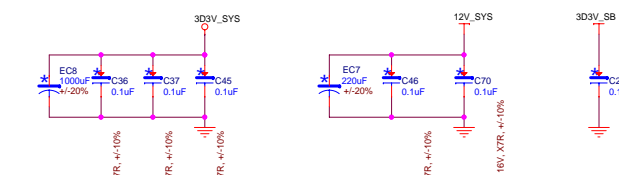
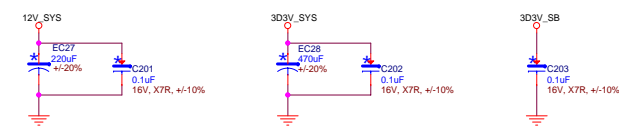
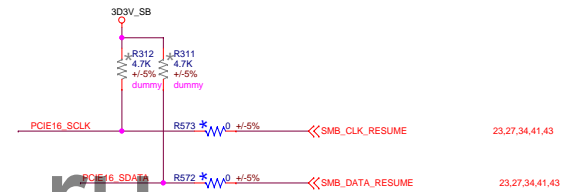
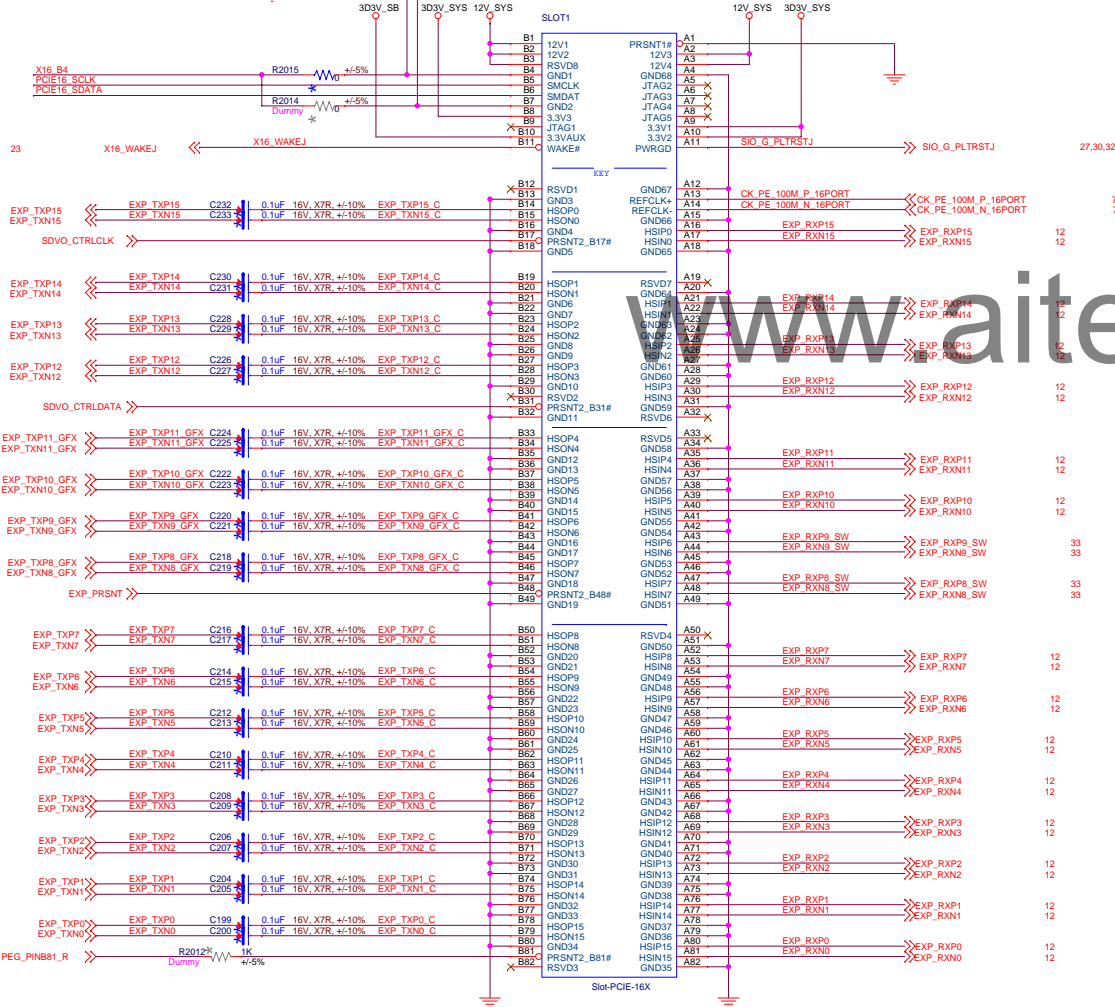
X16_B4

PEG_PINB7_R

R2011
8.2K
+/-5%

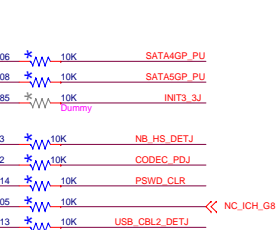
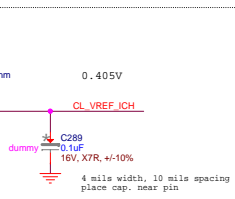
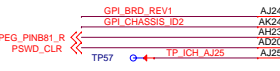
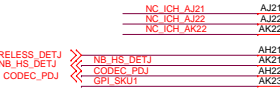
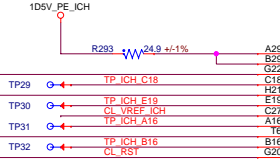
Dummy

Slot-PCIe 16X

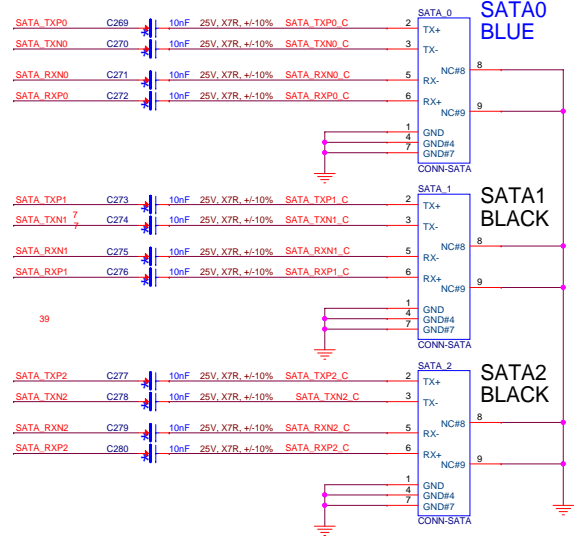
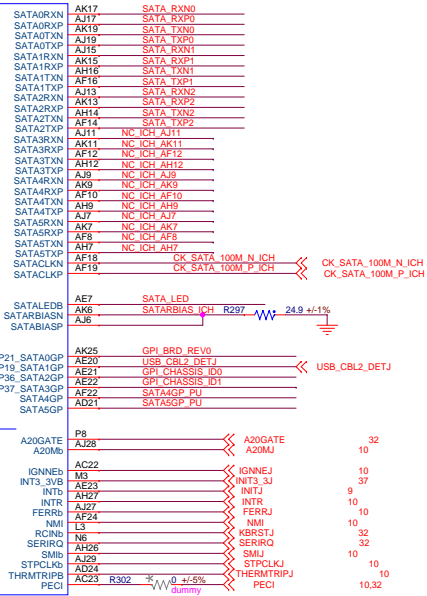


ICH10

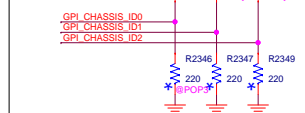
4 mile width, length no longer than 500 mile
Trace tied together close to pins.



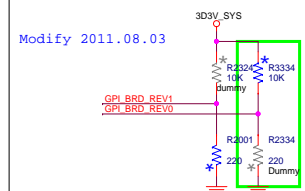
SATA



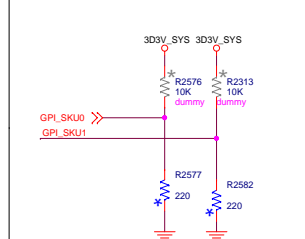
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0	0	1	DT
0	1	0	Reserved



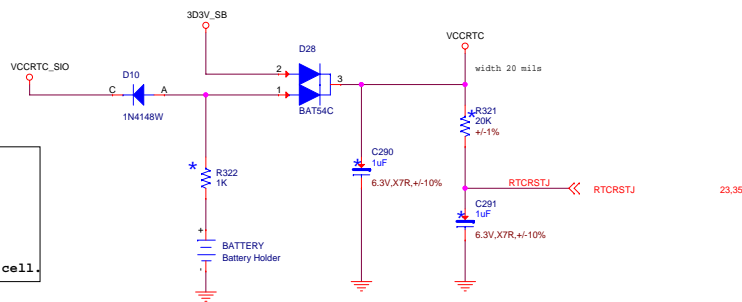
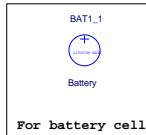
BOARD REV ID		
REV1	REV0	BOARD TYPE
0	0	Default
0	1	Reserved
1	0	Reserved
1	1	Reserved



SKU1	SKU0	BOARD TYPE
0	0	Default
0	1	Reserved
1	0	Reserved
1	1	Reserved



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INC.

Title

ICH10 -2

DWG NO

Telstra ERPII

Rev

A00

Date

Monday, May 21, 2012

Sheet

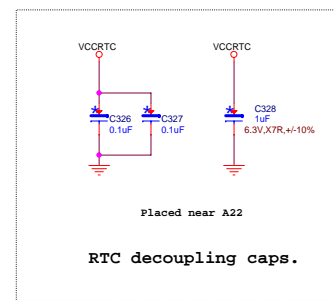
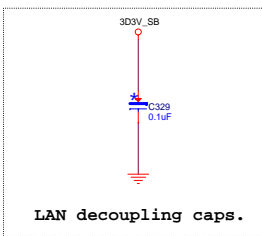
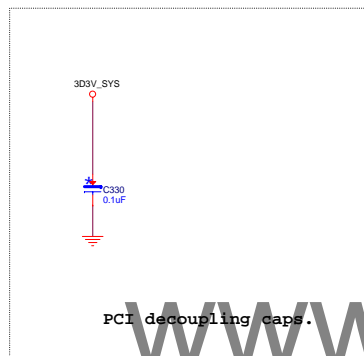
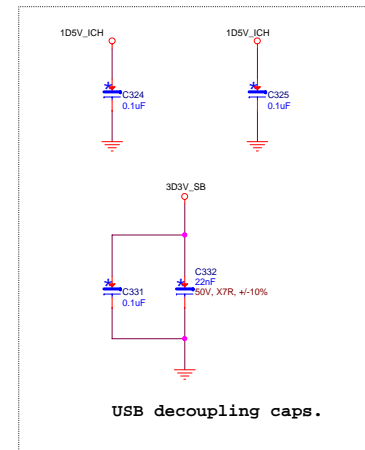
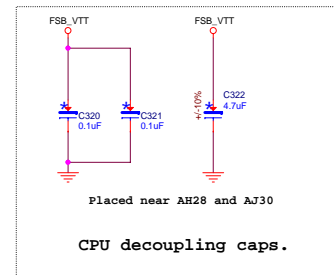
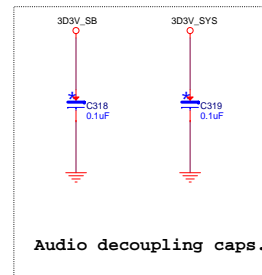
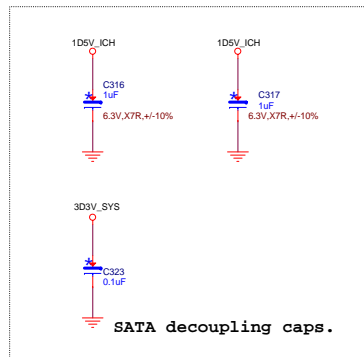
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of

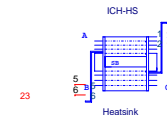
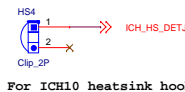
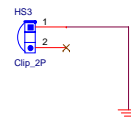
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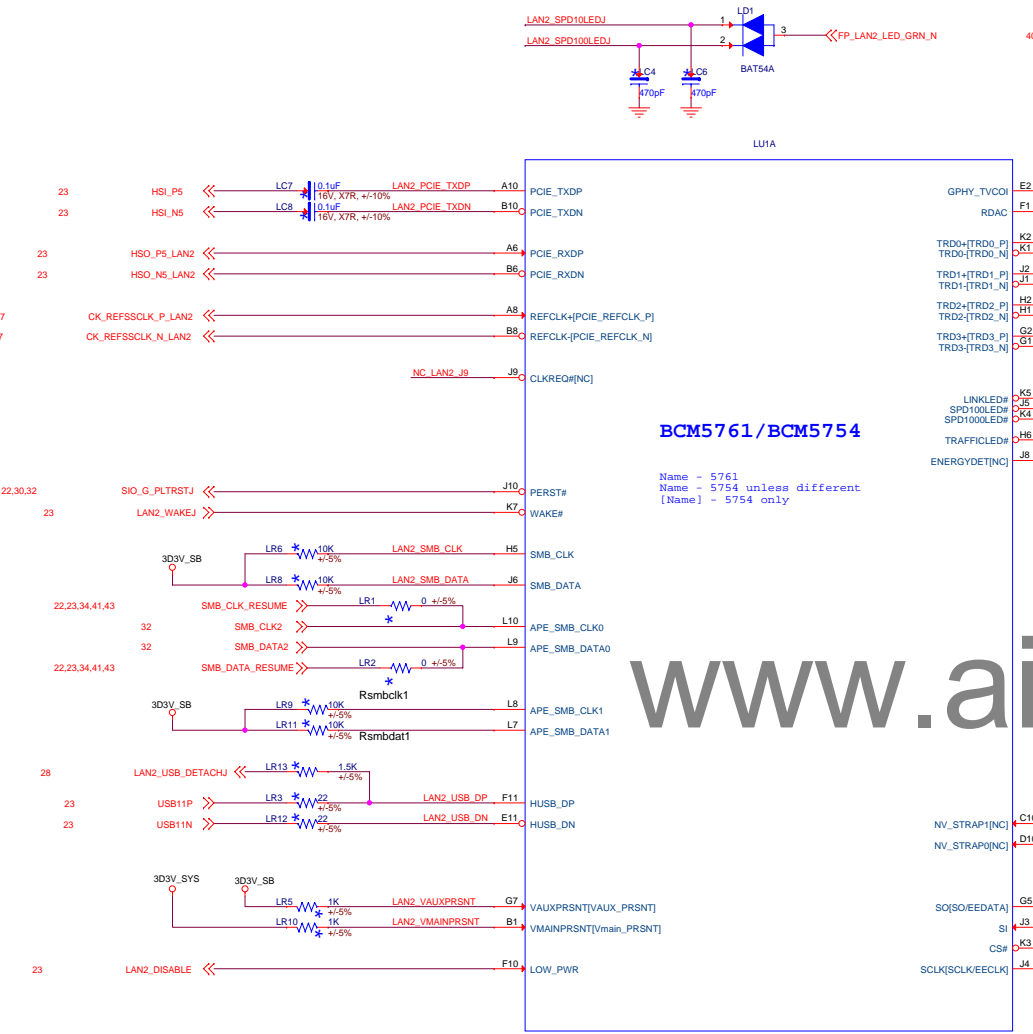


ICH10		
G30	VSS_100	H13
G29	VSS_101	H19
G25	VSS_102	H2
F6	VSS_103	H22
F5	VSS_104	H25
F28	VSS_105	H26
F26	VSS_106	H28
F21	VSS_107	H6
F12	VSS_108	VSS_092
E30	VSS_109	VSS_091
E29	VSS_110	VSS_090
E22	VSS_111	VSS_089
E2	VSS_112	VSS_087
E18	VSS_113	VSS_086
E15	VSS_114	VSS_085
D28	VSS_115	VSS_084
D25	VSS_116	VSS_083
D5	VSS_117	VSS_082
B28	VSS_118	VSS_081
B25	VSS_119	VSS_080
B22	VSS_120	VSS_079
B2	VSS_121	VSS_078
B19	VSS_122	VSS_077
B17	VSS_123	VSS_076
B14	VSS_124	VSS_075
B11	VSS_125	VSS_074
AK6	VSS_126	VSS_073
AK30	VSS_127	VSS_072
AK29	VSS_128	VSS_071
AK2	VSS_129	VSS_070
AK16	VSS_130	VSS_069
AK14	VSS_131	VSS_068
AK12	VSS_132	VSS_067
AJ8	VSS_133	VSS_066
AJ5	VSS_134	VSS_065
AJ26	VSS_135	VSS_064
AJ23	VSS_136	VSS_063
AJ20	VSS_137	VSS_062
AJ16	VSS_138	VSS_061
AJ14	VSS_139	VSS_060
AJ12	VSS_140	VSS_059
AH8	VSS_141	VSS_058
AH6	VSS_142	VSS_056
AH20	VSS_143	VSS_055
AH2	VSS_144	VSS_054
AH19	VSS_145	VSS_053
AH15	VSS_146	VSS_052
AH13	VSS_147	VSS_051
AG28	VSS_148	VSS_050
AF9	VSS_149	VSS_049
AF7	VSS_150	VSS_048
AF29	VSS_151	VSS_047
AF25	VSS_152	VSS_046
AF23	VSS_153	VSS_045
AF20	VSS_154	VSS_044
AF16	VSS_155	VSS_043
AF13	VSS_156	VSS_042
AE9	VSS_157	VSS_041
AE8	VSS_158	VSS_040
AE6	VSS_159	VSS_039
AE5	VSS_160	VSS_038
AE25	VSS_161	VSS_037
AE19	VSS_162	VSS_036
AE18	VSS_163	VSS_035
AE16	VSS_164	VSS_034
AE15	VSS_165	VSS_033
AE14	VSS_166	VSS_032
AE13	VSS_167	VSS_031
AE12	VSS_168	VSS_030
AE10	VSS_169	VSS_029
AE1	VSS_170	VSS_028
AD9	VSS_171	VSS_027
AD7	VSS_172	VSS_026
AD3	VSS_173	VSS_025
AD22	VSS_174	VSS_024
AD19	VSS_175	VSS_023
AD18	VSS_176	VSS_022
AD16	VSS_177	VSS_021
AD15	VSS_178	VSS_020
AD14	VSS_179	VSS_019
AC8	VSS_180	VSS_018
AC6	VSS_181	VSS_017
AC5	VSS_182	VSS_016
AC30	VSS_183	VSS_015
AC29	VSS_184	VSS_014
AC24	VSS_185	VSS_013
AC12	VSS_186	VSS_012
AC1	VSS_187	VSS_011
AB3	VSS_188	VSS_010
AB28	VSS_189	VSS_009
AB26	VSS_190	VSS_008
AA6	VSS_191	VSS_007
AA5	VSS_192	VSS_006
AA27	VSS_193	VSS_005
AA29	VSS_194	VSS_004
AJ4	VSS_195	VSS_003
AF3	VSS_196	VSS_002
B27	VSS_197	VSS_001
B27	VSS_198	A1

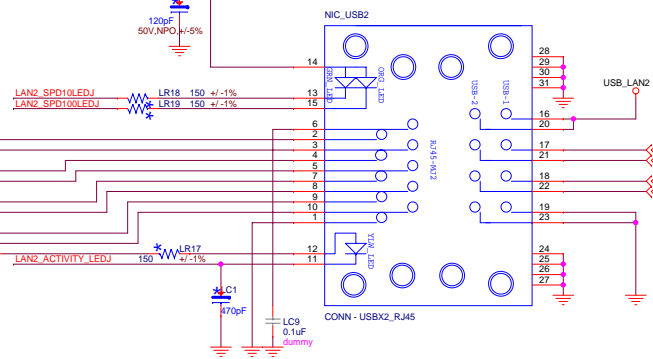


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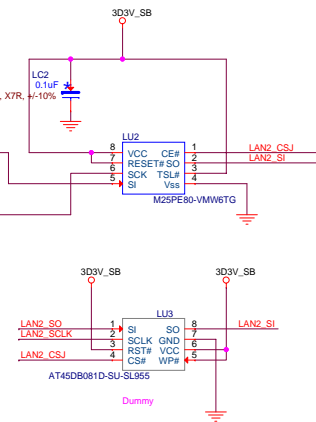




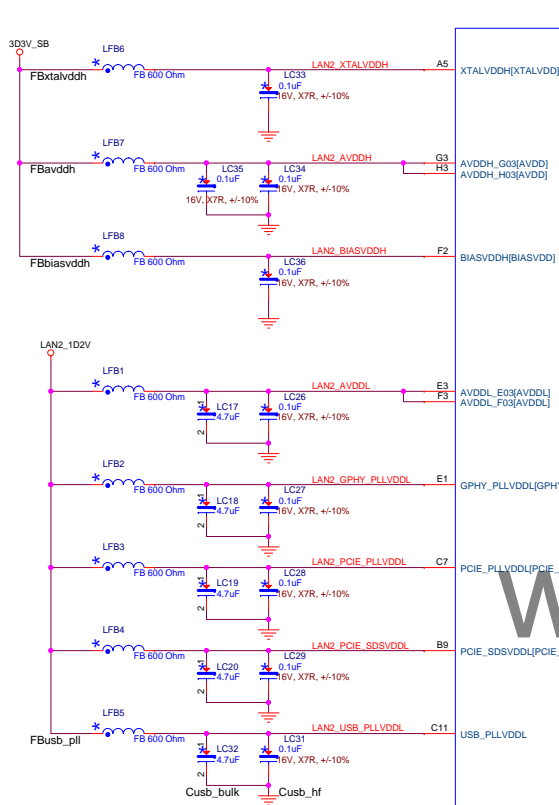
PHY_TVCOI
RDAC
K2 LAN2 TRD0_P
K1 LAN2 TRD0_N
J2 LAN2 TRD1_P
J1 LAN2 TRD1_N
H2 LAN2 TRD2_P
H1 LAN2 TRD2_N
G2 LAN2 TRD3_P
G1 LAN2 TRD3_N
K5 LAN2 SPD10LEDJ
J5 LAN2 SPD100LEDJ
K4 NC LAN2_K4
H6 LAN2 ACTIVITY LEDJ
J8 NC LAN2_J8
LINKLEDJ
SPD100LEDJ
SPD100LEDJ
TRAFFICLEDJ
ENERGYDET[NC]



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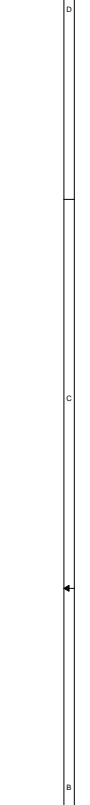
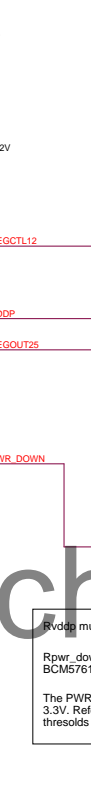
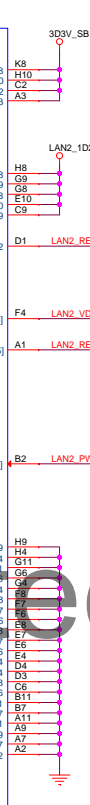


LU3 is LU2 second source
If pop LU3, must dummy LU2



BCM5761/BCM5754

Name - 5761
Name - 5754 unless different
[Name] - 5754 only



If the BCM5761 is installed, Fusb_pll, Cusb_bulk and Cusb_hf must be laid out even if the USB interface is not used since the USB PLL may provide an alternate clock source internal to the BCM5761.

If the BCM5754 is installed, Fusb_pll, Cusb_bulk and Cusb_hf may be uninstalled.

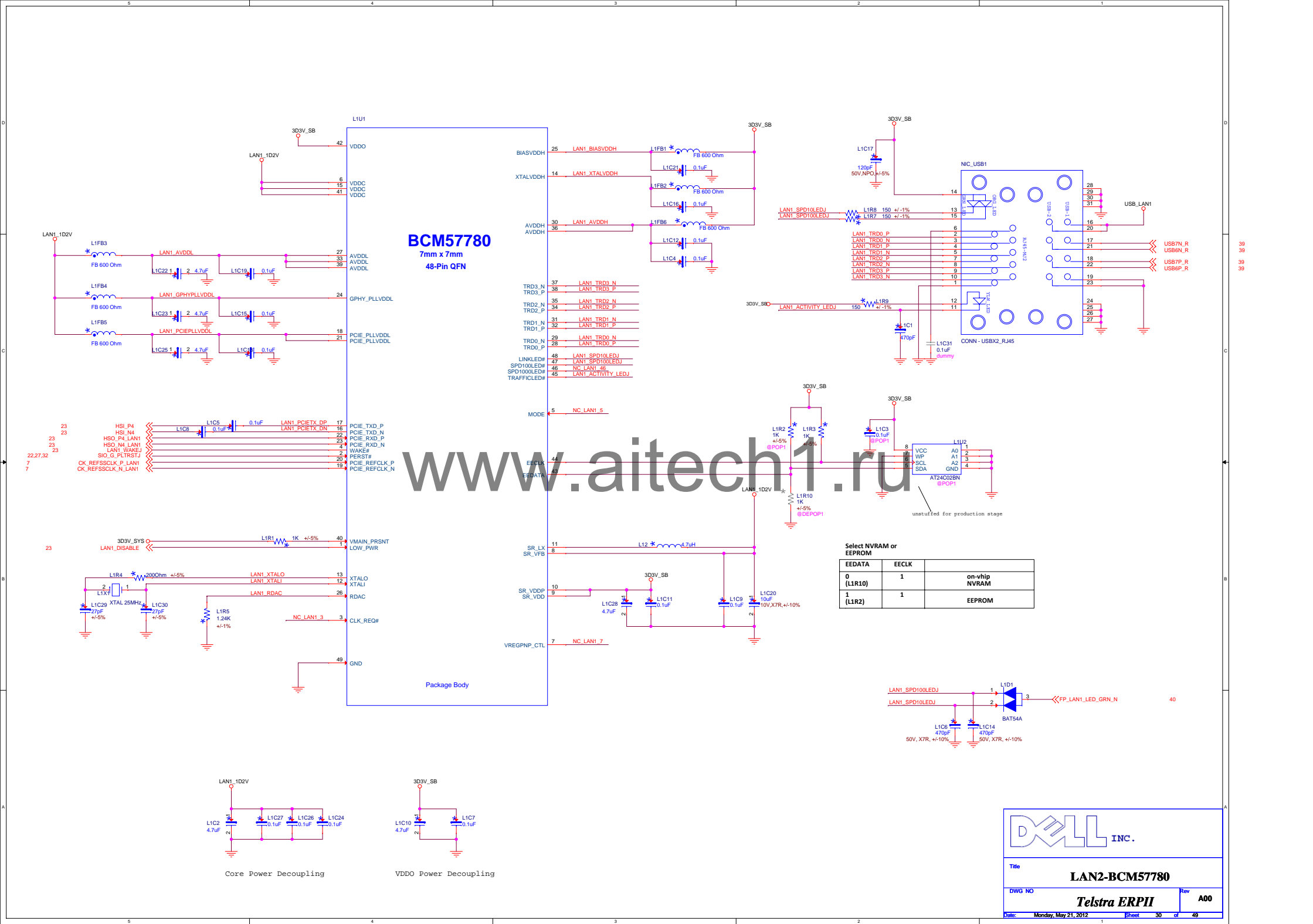
Rvddp must be installed with the BCM5754 only.

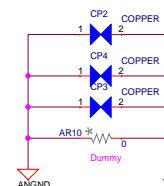
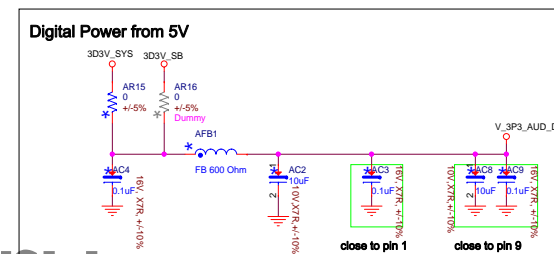
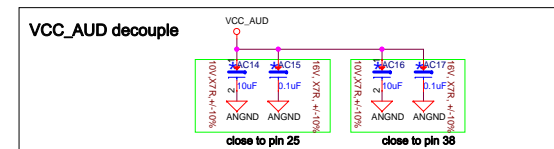
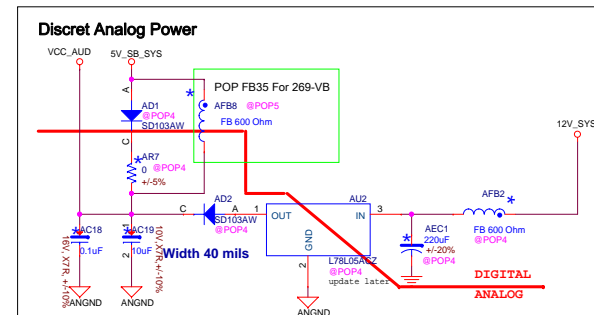
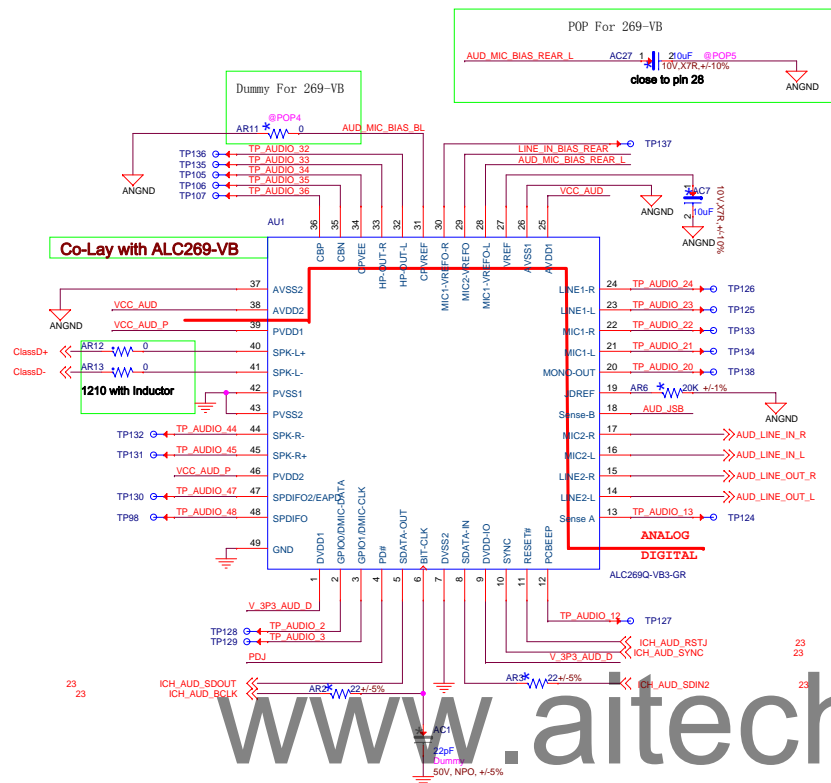
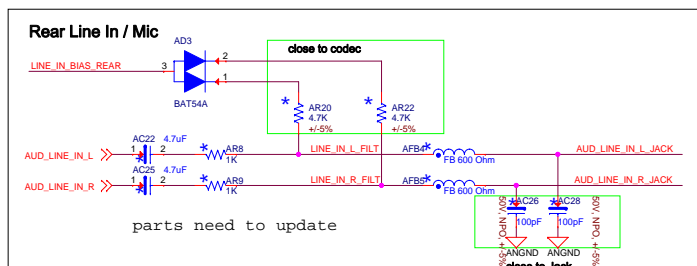
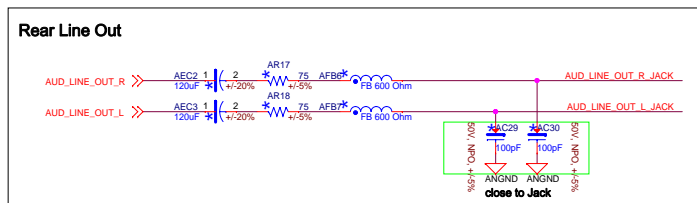
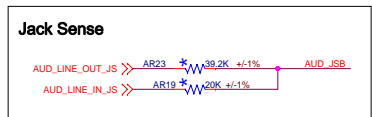
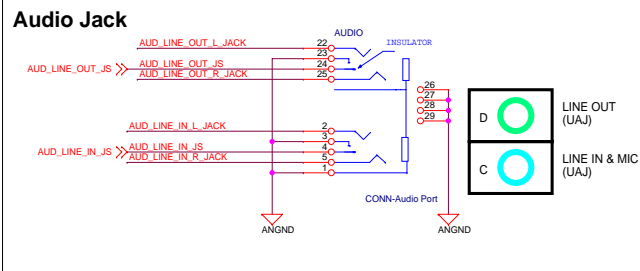
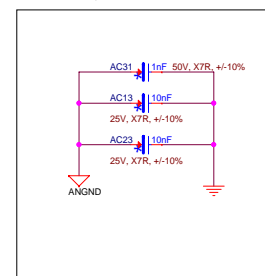
Rpwr_down_pd must be installed with the BCM5761 only.

The PWR_DWN[VDDP] ball must not be driven to 3.3V. Refer to the BCM5761 data sheet for logic thresholds and maximum ratings.

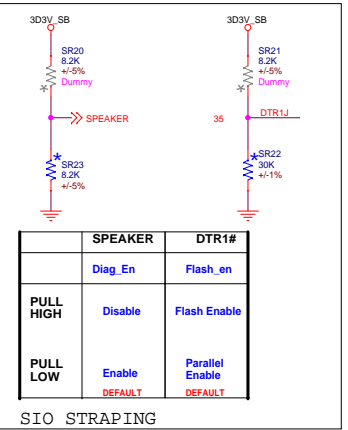
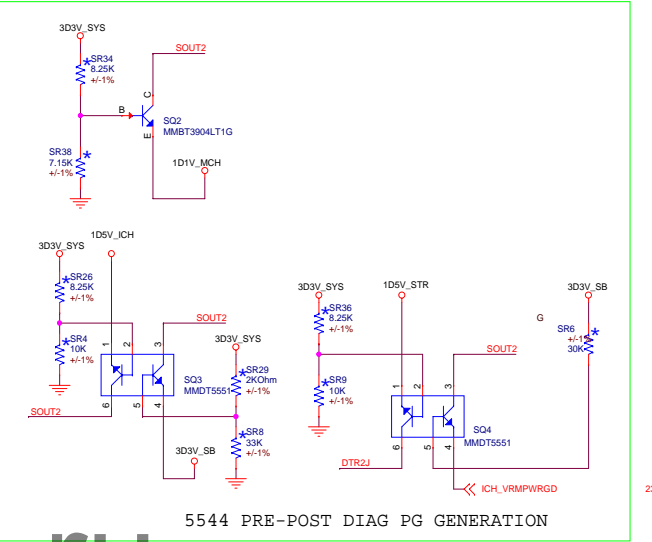
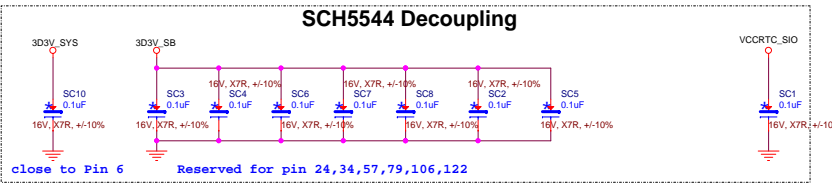
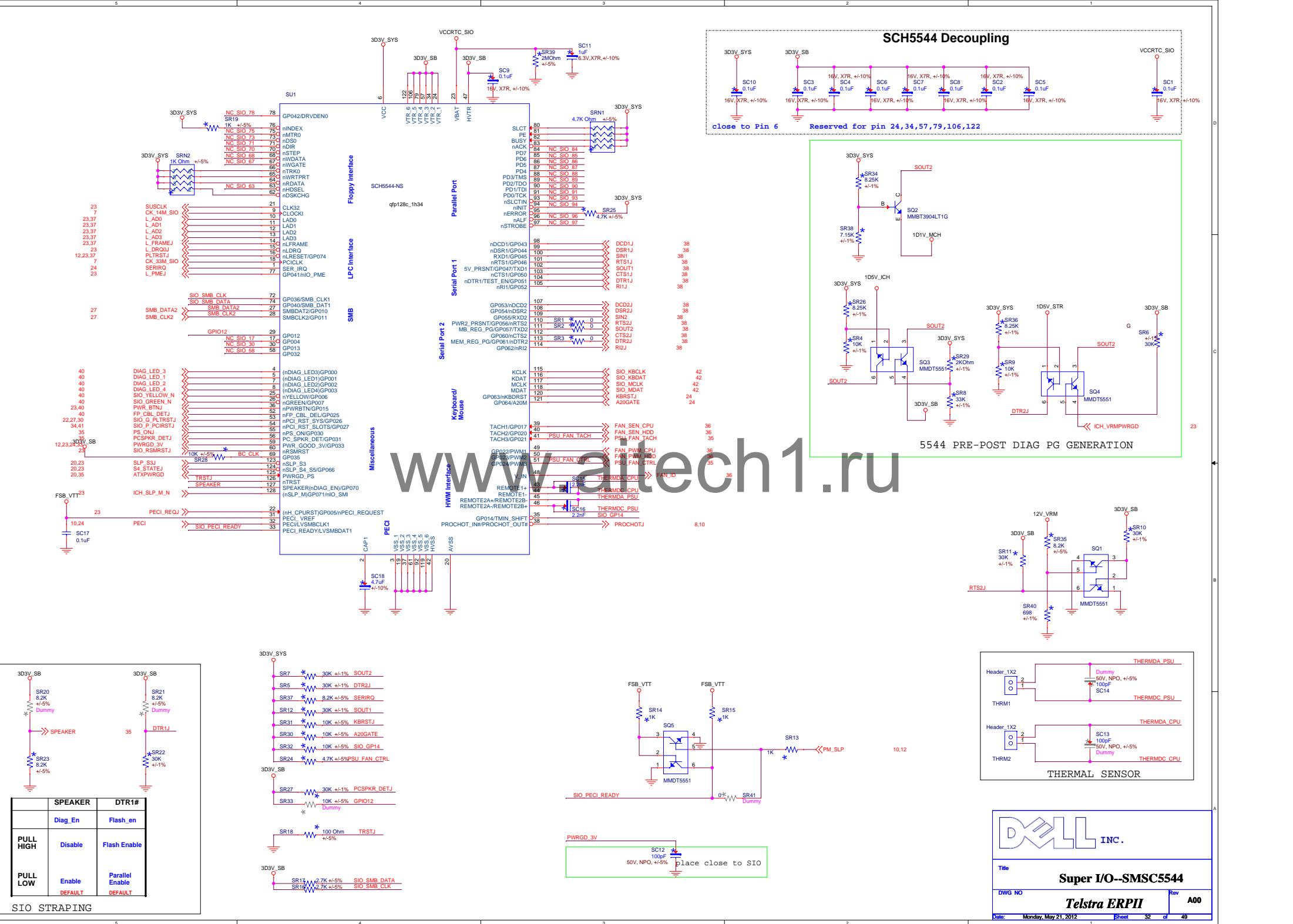


Title	LAN1-BCM5761_3	
DWG NO	Telstra ERPII	
Date	Monday, May 21, 2012	Sheet 29 of 49
Rev	A00	

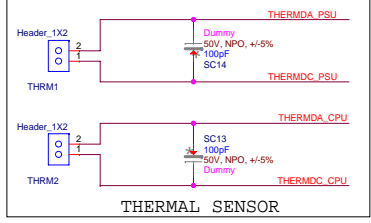
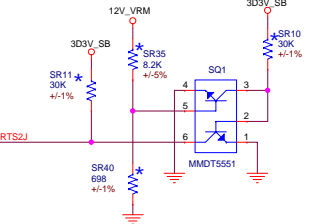
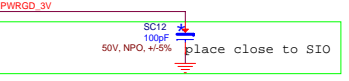
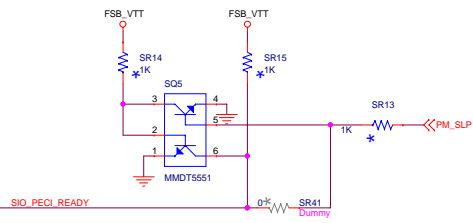


**Stitch Cap.**

For Vista Premium spec (and for CODEC reliability in general), need to have very low impedance connection between AGND and DGND right at CODEC. ADI recommend a copper trace about 80 mils wide under CODEC (on the GND layer), bridging the two planes across the moat.



	SPEAKER	DTR1#
	Diag_En	Flash_en
PULL HIGH	Disable	Flash Enable
PULL LOW	Enable	Parallel Enable
	DEFAULT	DEFAULT



Title

Super I/O-SMSC5544

DWG NO

Telstra ERPH

Date

Monday, May 21, 2012

Rev

A00

Sheet

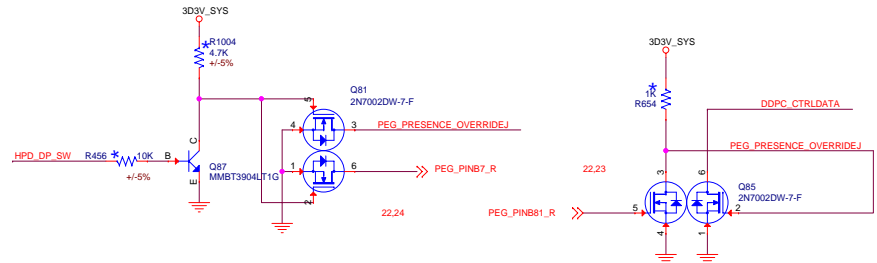
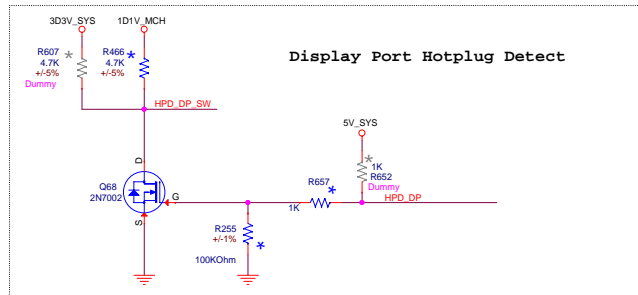
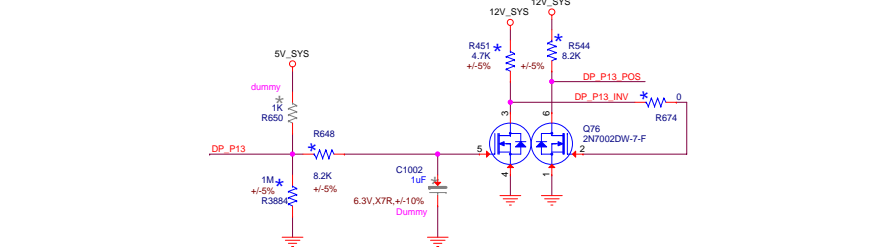
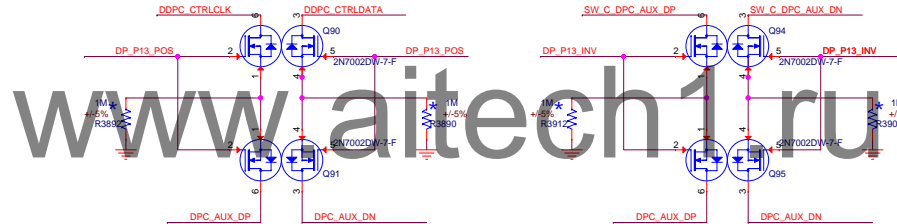
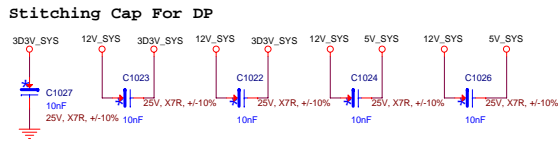
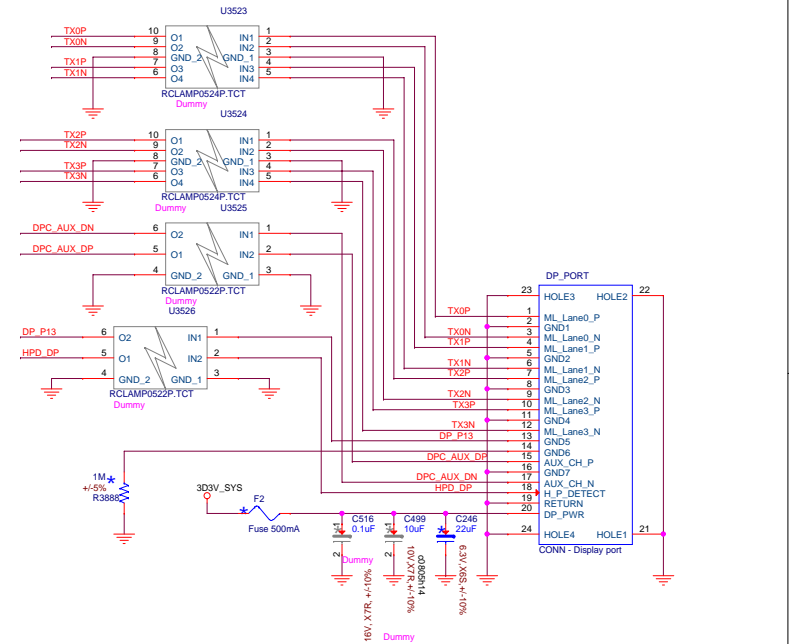
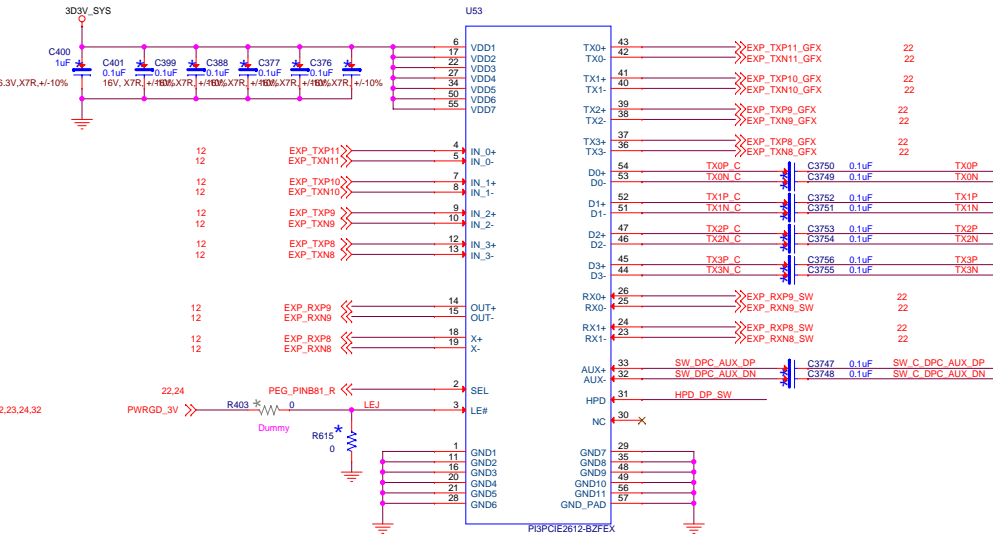
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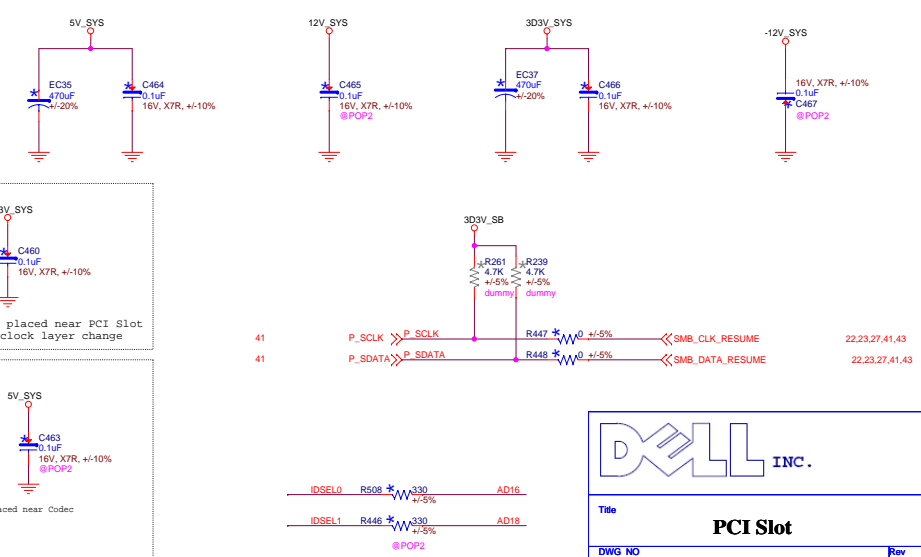
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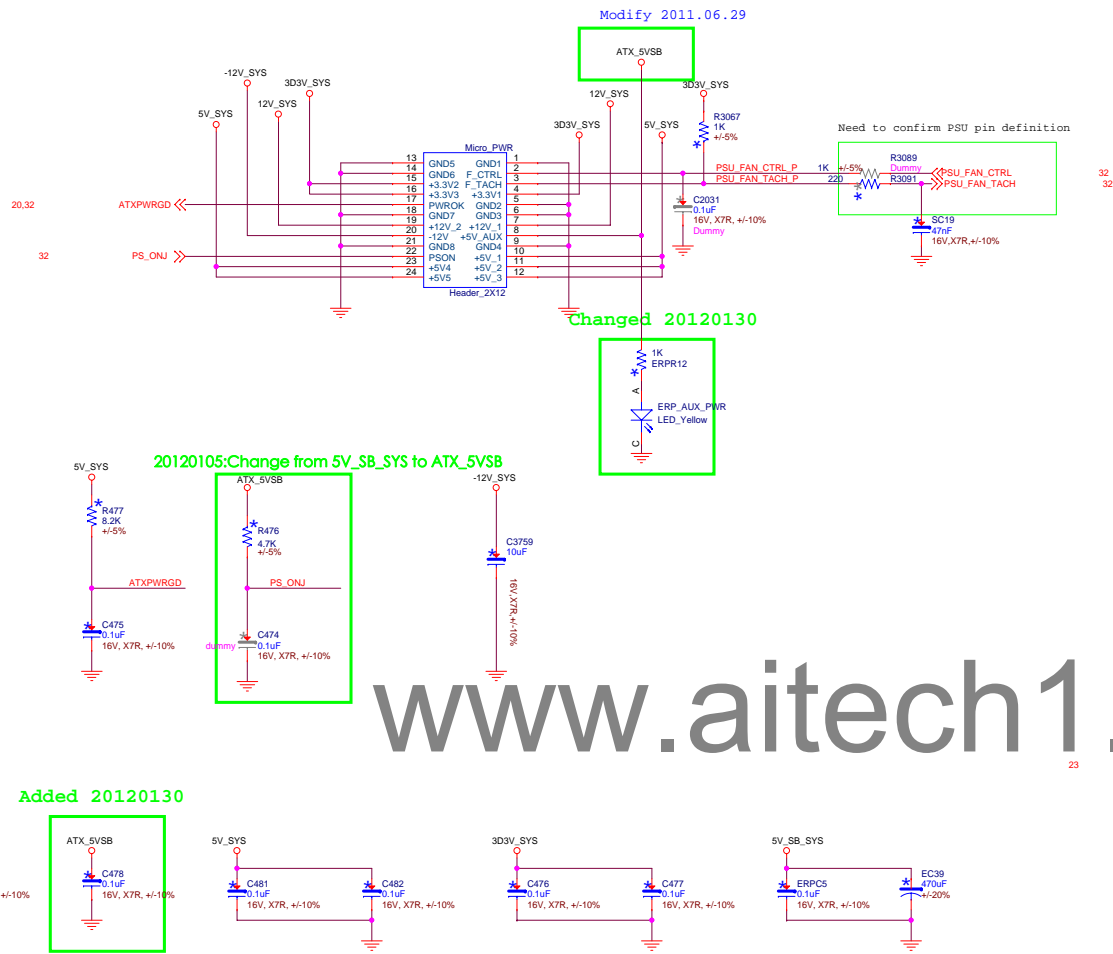
49

GENII SWITCH

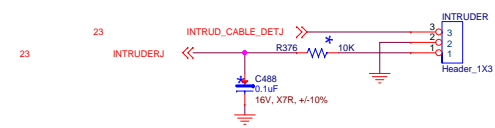
DISPLAY PORT







Chassis Intruder Header



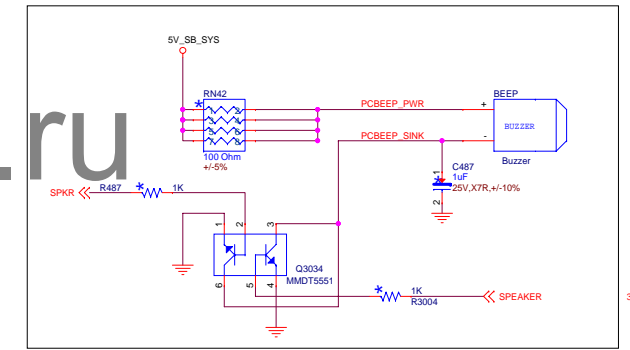
Clear CMOS

1-2: CLEAR CMOS
EMPTY: NORMAL

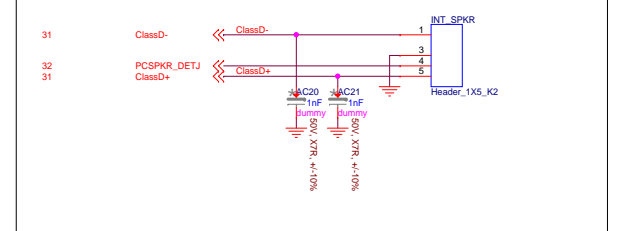


Clear Password

1-2: NORMAL
EMPTY: CLEAR PASSWORD



Internal Speaker



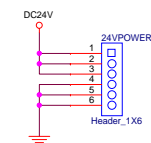
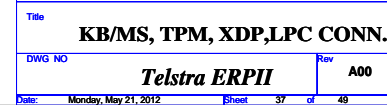


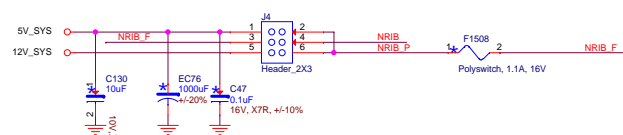
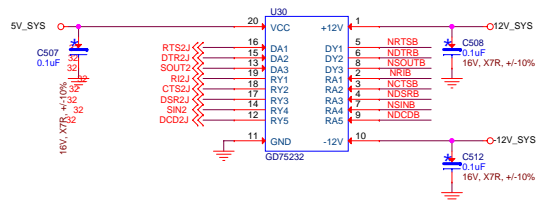
BTX, PRT, MISC Connector

Telstra ERPII

Rev **A00**

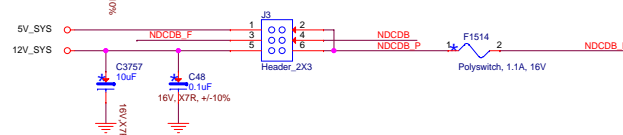
Date: Monday, May 21, 2012 Sheet 35 of 49

[illegible][illegible]



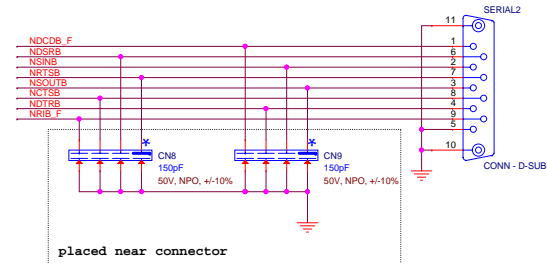
1-2: 5V
3-4: RI
5-6: 12V

J4_JUMPER(3-4)
Jumper_2P_Blu

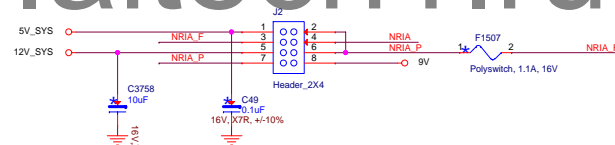
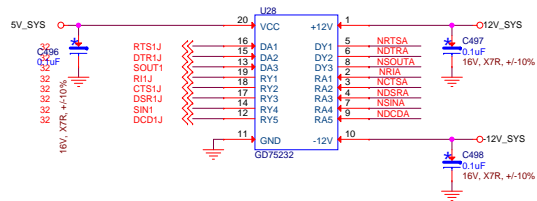


1-2: 5V
3-4: DCD
5-6: 12V

J3_JUMPER(3-4)
Jumper_2P_Blu

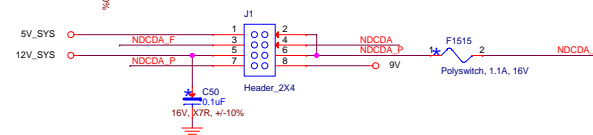


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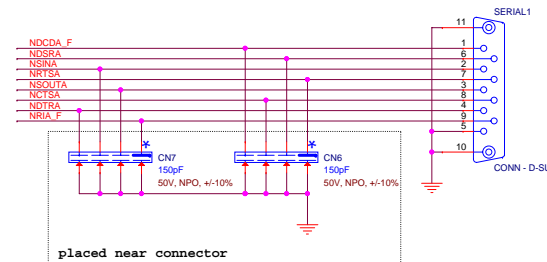
1-2: 5V
3-4: RI
5-6: 12V
7-8: 9V

J2_JUMPER(3-4)
Jumper_2P_Blu

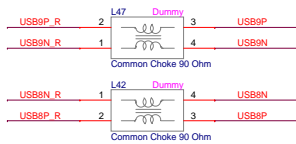
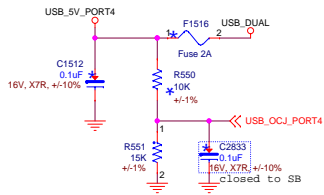
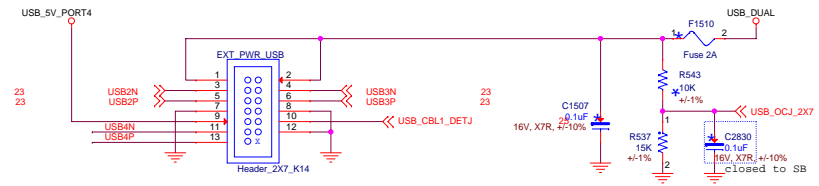
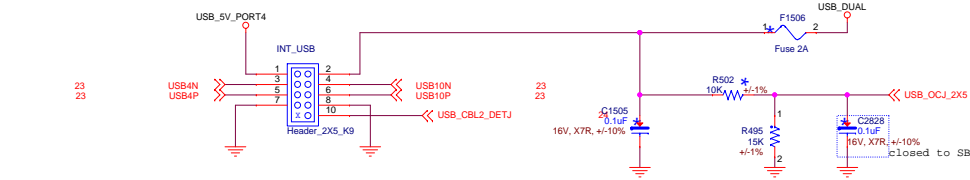


1-2: 5V
3-4: DCD
5-6: 12V
7-8: 9V

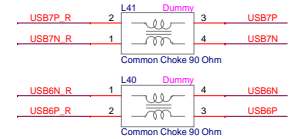
J1_JUMPER(3-4)
Jumper_2P_Blu



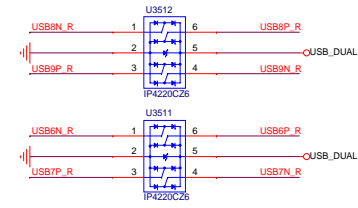
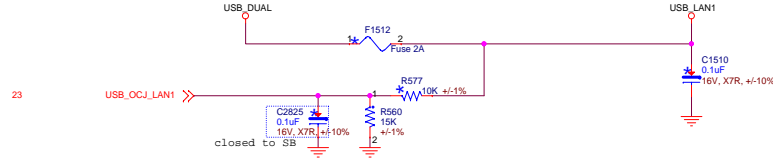
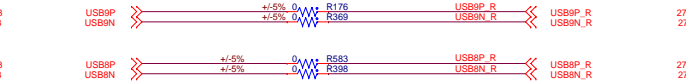
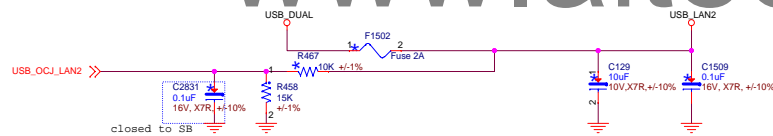
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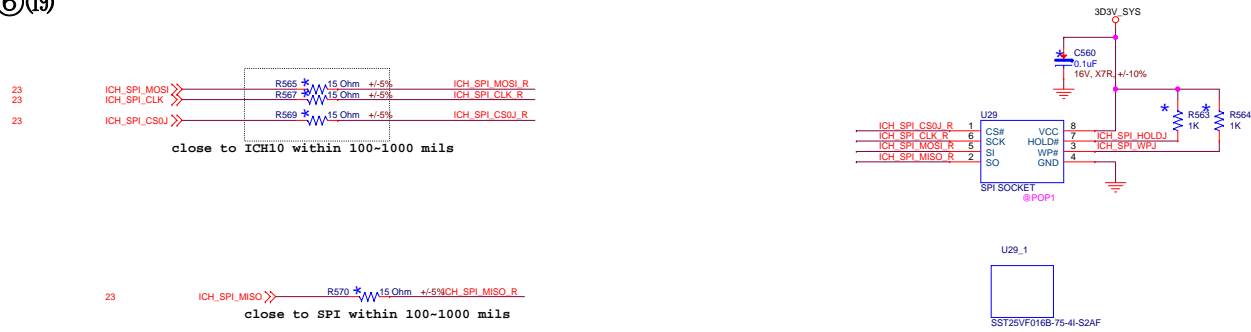
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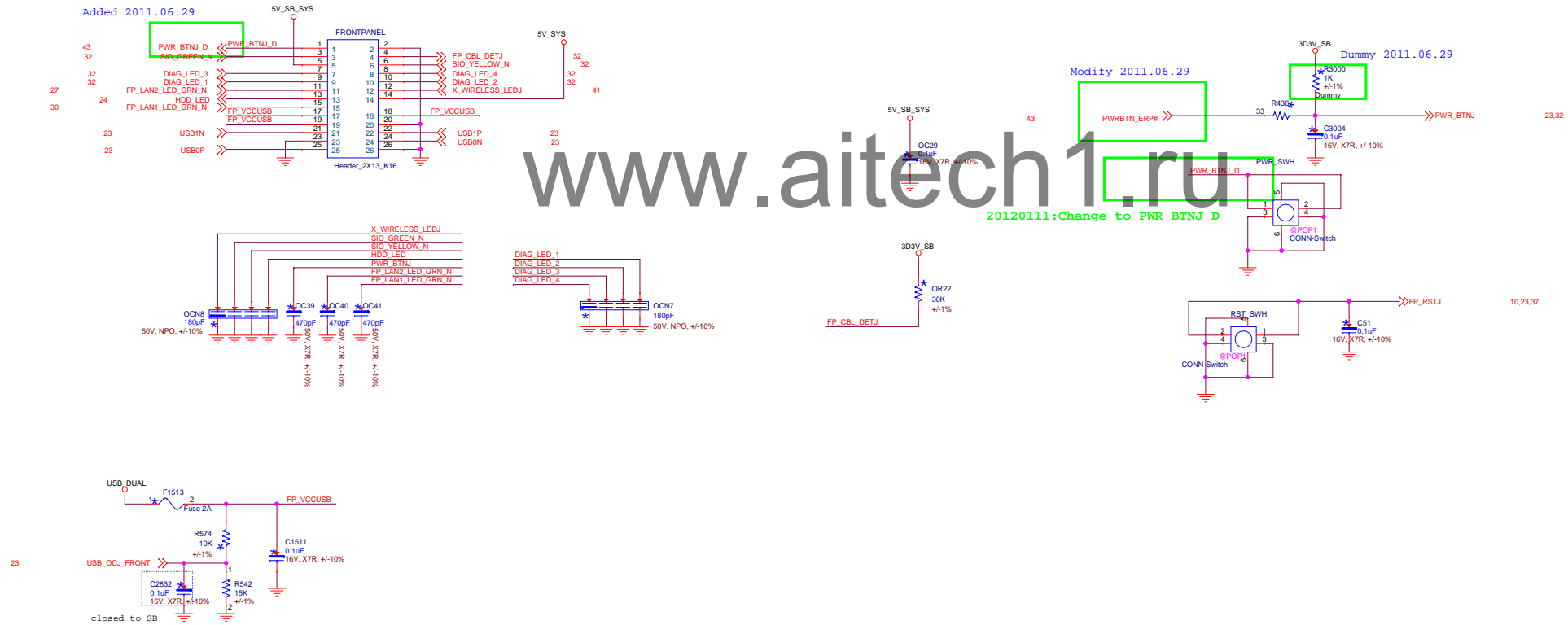
CO-LAY with Four 0603 Serial Resistors



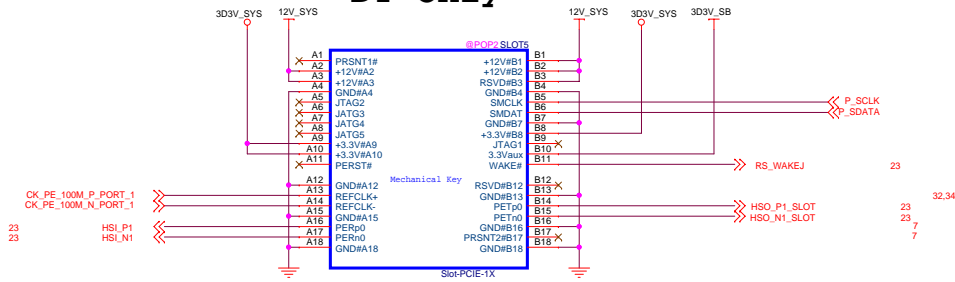
6(19)



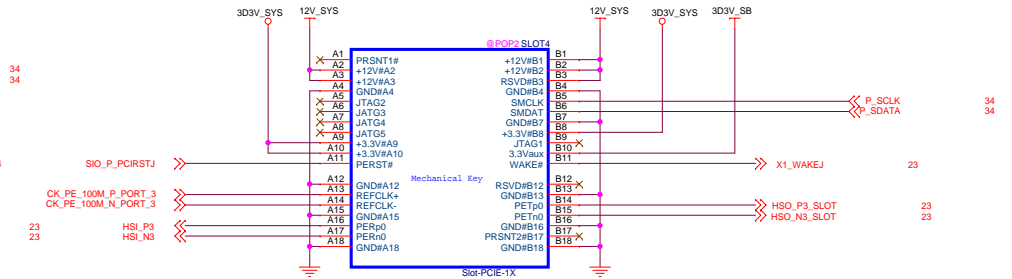
(16) 8 5 4 10 6 11 4 15 2



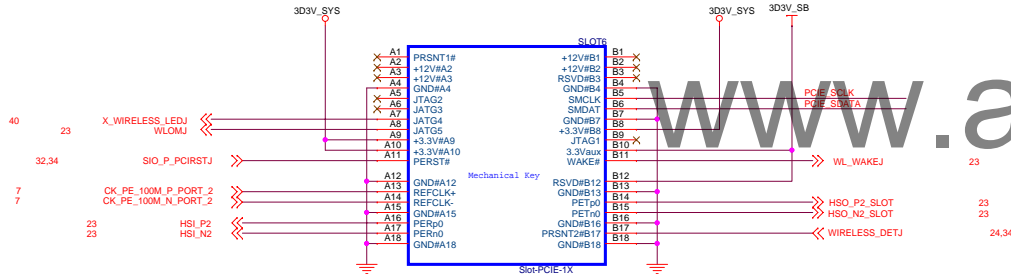
Riser DT Only



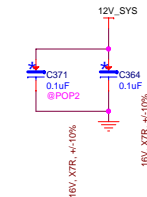
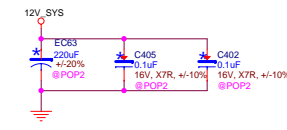
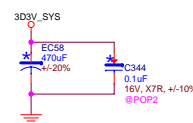
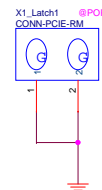
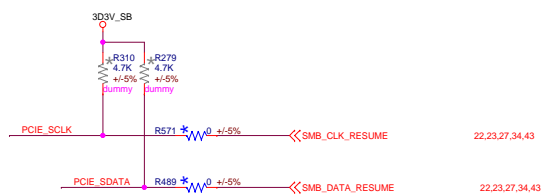
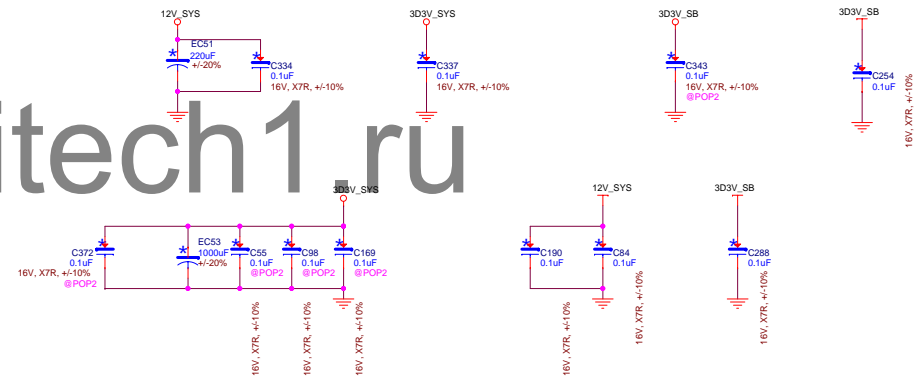
PCIe X1 DT Only



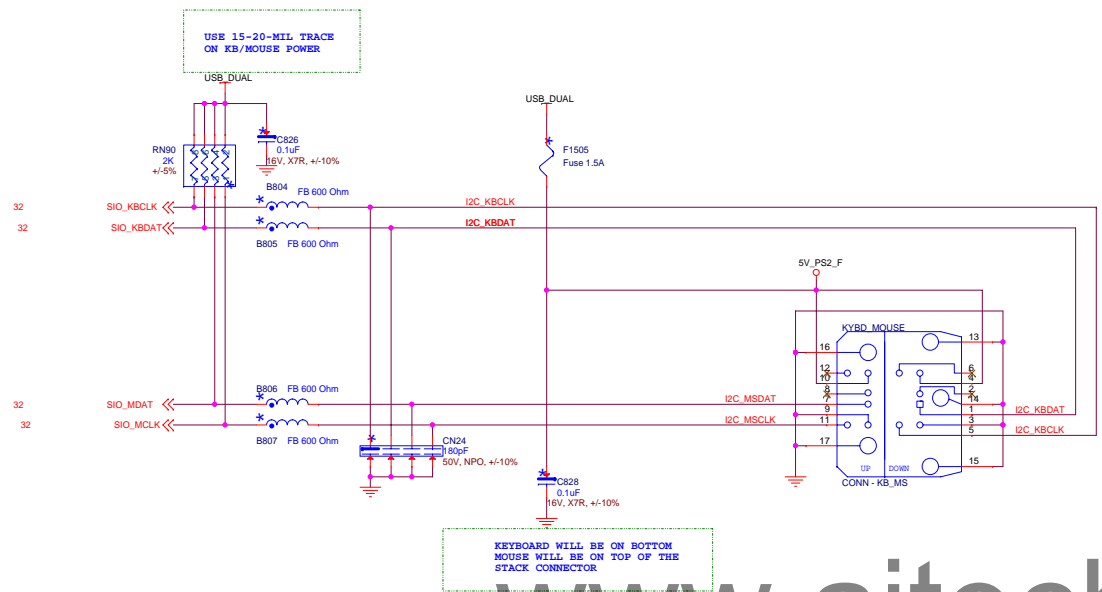
Wireless



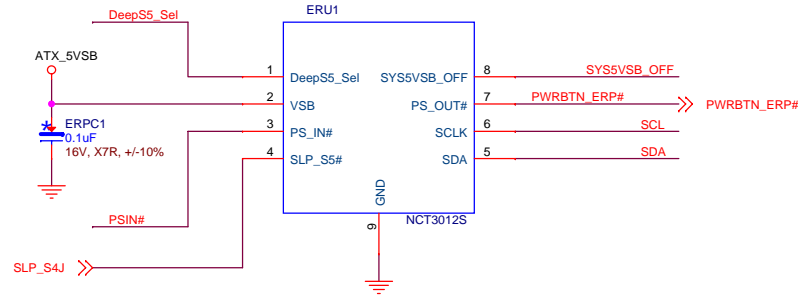
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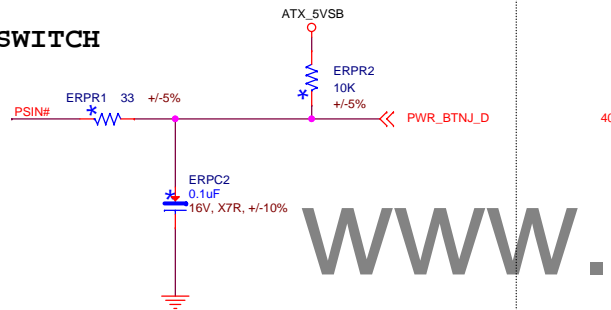
KB / MS + COM2 Connector



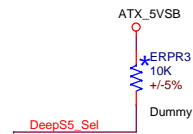
nuvoTon



PANEL SWITCH

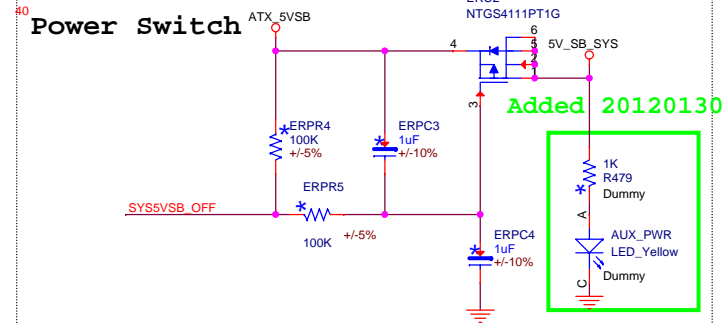


Strapping PIN

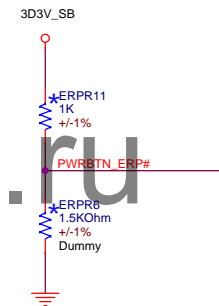


DeepS5_Sel:
Delay 6 seconds to enter Deep S5 at the first power on: Pull-high 10k.
Do not enter Deep S5 at the first power on: Floating (Internal Pull-Down).

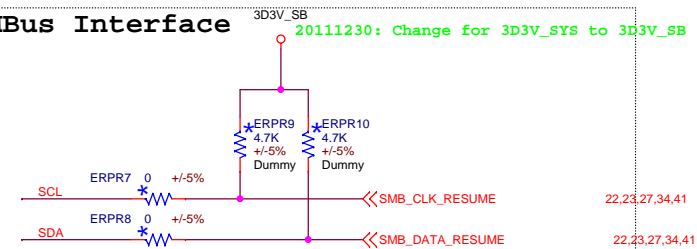
Power Switch



Pull-High



SMBus Interface



DELL INC.

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ERP 0.5 W Solution

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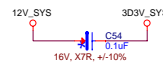
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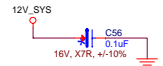
Sheet 43 of 49

Stitching Cap

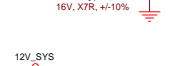
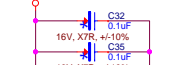
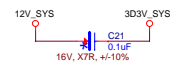
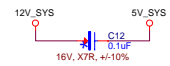
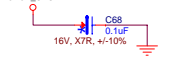
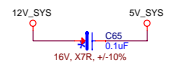
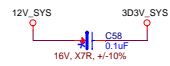
FOR CK_33M_DEBUG



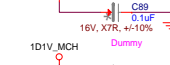
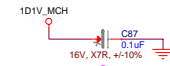
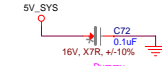
FOR Internal USB



FOR PCI

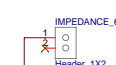
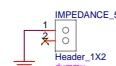
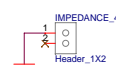
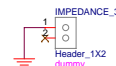
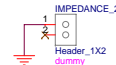
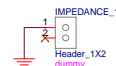
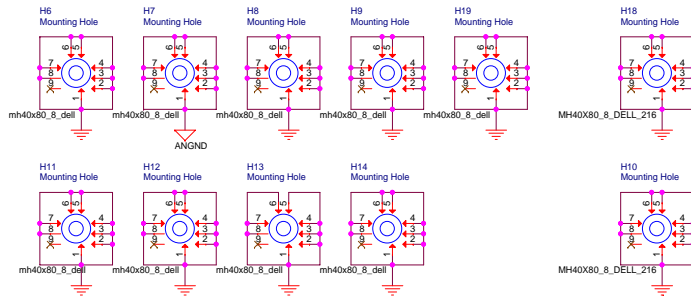


Request for Dell EMC feedback on 0512



DDR TEST POINT DIP

TP101 TP102



Title
Reserved

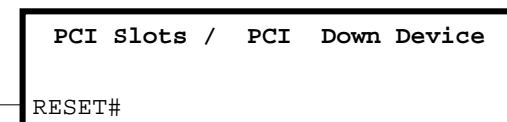
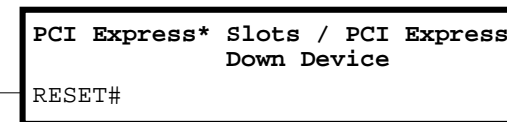
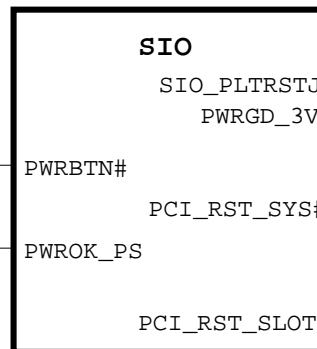
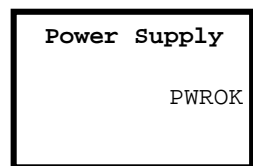
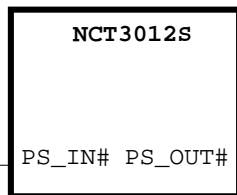
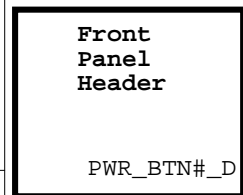
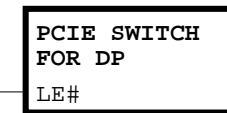
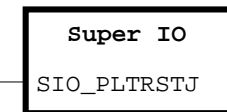
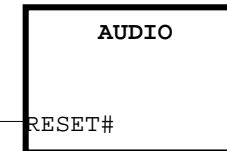
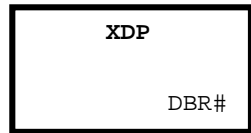
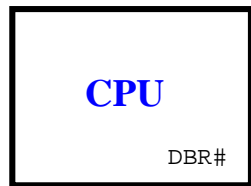
DWG NO
Telstra ERPII
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PCI Routing Summary

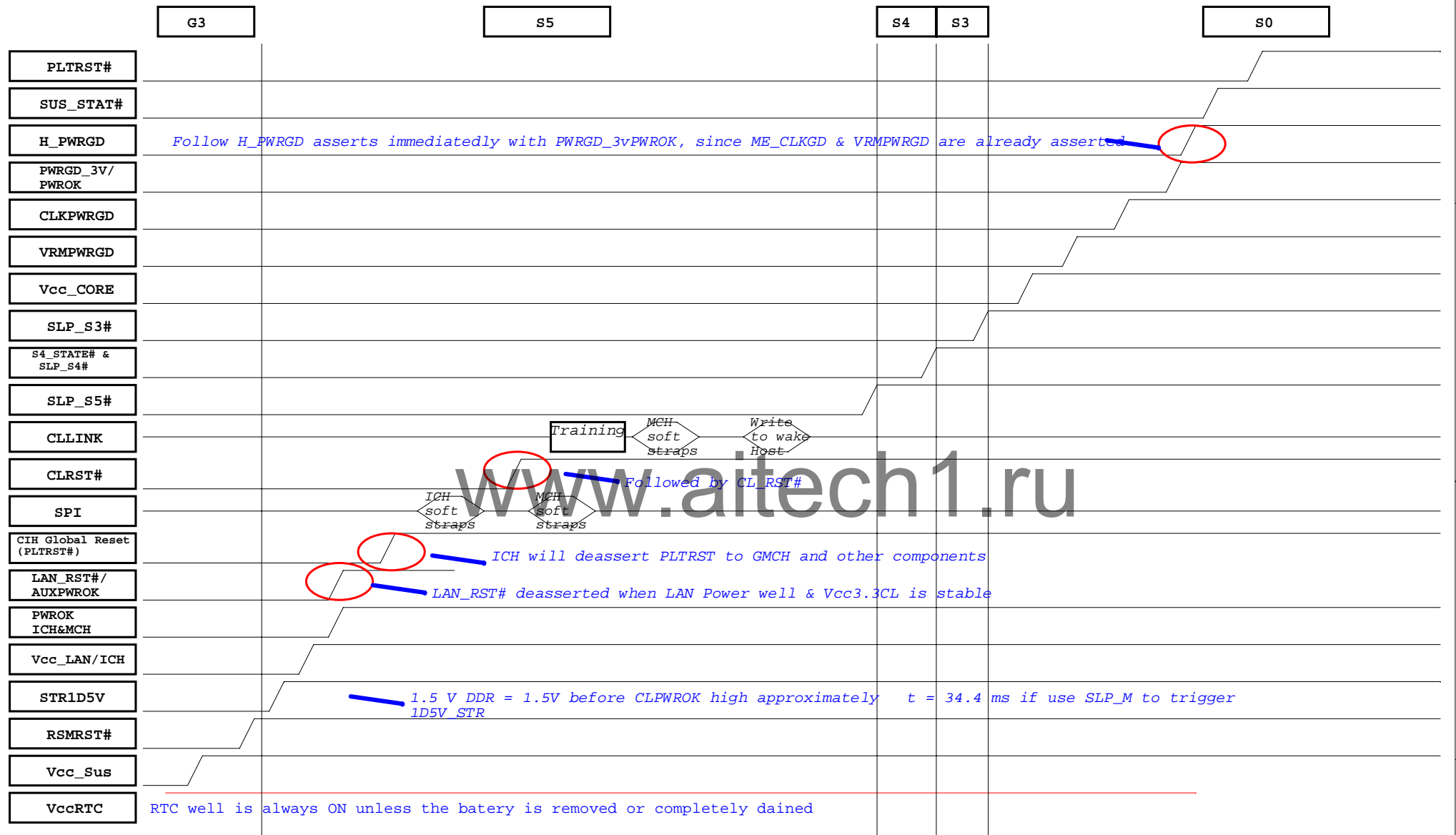
	PCI0	PCI1				
INTAJ	A	C				
INTBJ	B	D				
INTCJ	C	A				
INTDJ	D	B				
INTEJ						
INTFJ						
INTGJ						
INTHJ						

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Title RESET MAP		
DWG NO	Rev	
	Telstra ERPII A00	
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Clock Gen Seligo SLG8XP523TTR Functional Straps

PIN NAME	NET		Strapping description
PCI2/TME (PIN4)	CK_PIN4	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI3/CFGF (PIN5)	CK_PIN5	1	CGF TABLE ENABLED
		0	CGF TABLE DISABLED
PCI4/SRC5_EN (PIN6)	CK_PIN6	1	SRC5
		0	CPU_STOP# and PCI_STOP# DEFAULT
PCI_F5/ITP_EN (PIN7)	CK_PIN7	1	CPU_ITP
		0	SRC8 DEFAULT

SIO SMSC5544 Functional Straps

PIN NAME	NET		Strapping description
SPEAKER[DIAG_EN#] /GP8051_45/GP14 (PIN127)	SPEAKER	1	Diag_En Disable
		0	Diag_En Enable DEFAULT
DTR1#[FLASH_EN] /GP8051_16 (PIN104)	DTR1#	1	Flash Enable
		0	Parallel Enable DEFAULT

Intel ICH10 Functional Straps

PIN NAME	NET		Strapping description
TP3	TP28	1	Danbury Technology Enable Internal Pull-up
		0	XOR Chain Entrance
SPKR	SPKR	1	NoReboot mode
		0	Reboot mode Internal Pull-down
GPIO33	MFG_MODE	1	ME enable DEFAULT
		0	ME disable
SPI_MOSI	ICH_SPI_MOSI	1	MCH TPM Enable
		0	MCH TPM disable DEFAULT Foalt

Intel MCH Eaglelake Q45 Functional Straps

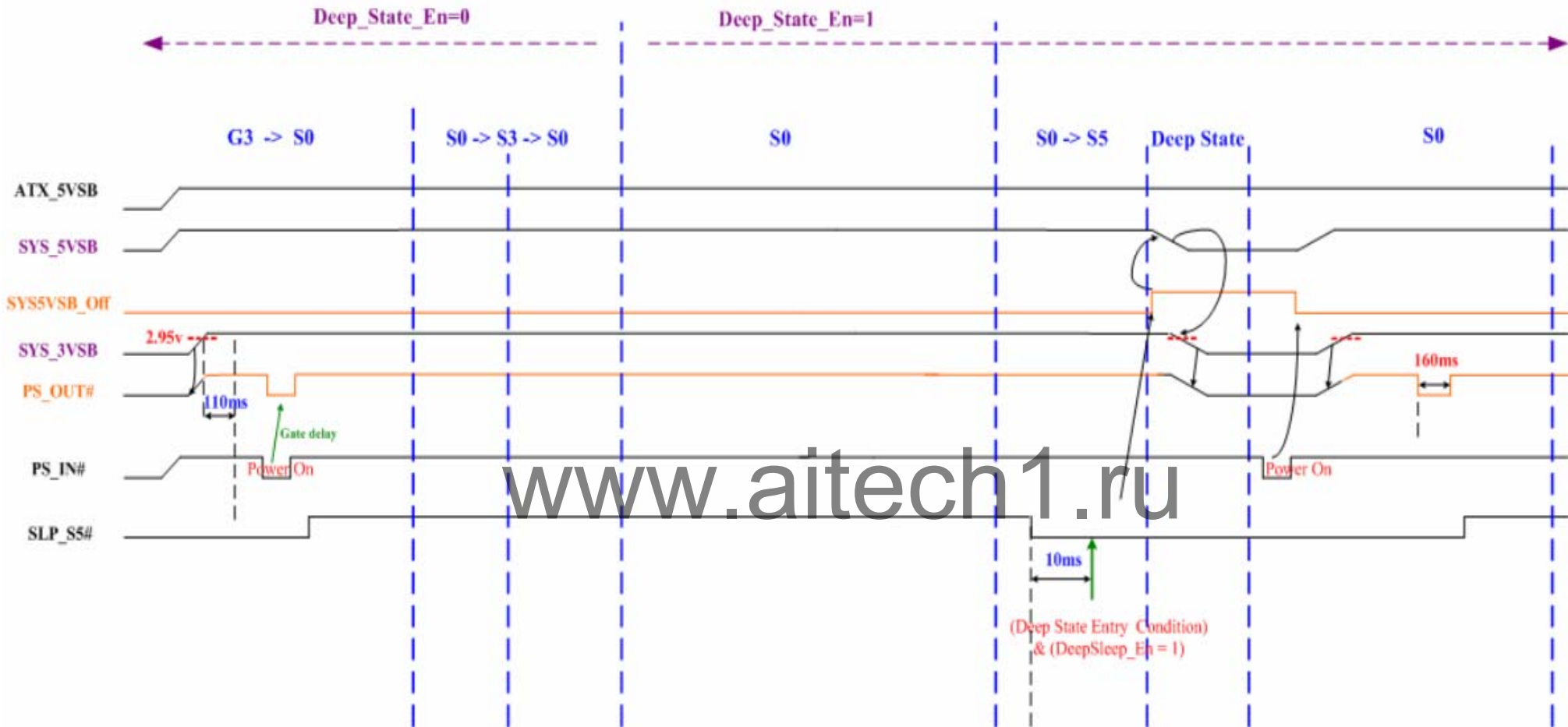
PIN NAME	NET		Strapping description
cen	TLS	1	TLS Enable
		0	TLS disable DEFAULT
iTPMb	ITPM_EN	1	iTPM disable DEFAULT Foalt
		0	iTPM Enable
DDPC_CTRLDATA	DDPC_CTRLDATA	1	SELECT Display Port
		0	SELECT PCIe X16
DDPC_CTRLCLK	DDPC_CTRLCLK	1	SELECT Display Port
		0	SELECT PCIe X16

NCT3012S Functional Straps

PIN NAME	NET		Strapping description
DeepS5_Sel	DeepS5_Sel	1	Delay 6 seconds to enter Deep S5 at the first power on
		0	Do not enter Deep S5 at the first power on DEFAULT



Power Sequence of NCT3012S



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PS : => Black : Input pin ; Orange : Output pin ; Purple : System signal



Title

Power sequence of NCT3012S

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B00 TO X00 change list

4/30
Page 31 add AR24 .0ohm for Audio PD# option , connect to ICH10 GPIO6
Page 39 add C129 .10uF in USB_LAN1
Page 25 change R1385 from 27K to 10Kohm
Page 30 add L1R1 , 10K for disable ext EEPROM

5/4
Page 38 CN9 swap pin
Page 23 dummy R307,R3114 and add R278 (10K)
Page 27 del LC5,LR16
Page 30 del L1R6,L1C18
Page 28 LAN1 swap pin
Page 32 change SC15,SC16 footprint to 0402

5/5
Page19
1. Change PQ20 PQ22 from ON NTD40N03 to AOS AOD452
2. Change 1D5V_ICH power source from DDR to 3D3V_SYS and DDR(dummy)
Page20
1. Change PQ14 PQ15 PQ31 from ON NTD40N03 to AOS AOD452
2. Add PEC25 470uF (dummy)

5/6
1. Page 43 add C53 for USB11
2. Page 35 change C487 from 0.1uF to 1uF

5/7
1. Page 37 add C2 for 24V
2. Page 40 U29 pin8 change connection from 3D3V_SB to3D3V_SYS
3. Page 19 dummy PRN1 , mount PRN2
4. change IMPEDANCE_1 and IMPEDANCE_3's connection to GND

5/8
1. Page 25 change ICH10 pin A12,B12,B23,C23 (VccCL_3.3V and VccLAN_3.3V) connection from 3D3V_SB to 3D3V_SYS
2. Page 43 del TP99 , TP100 , TP101 , TP102
3. Page 37,38 update parts L40,L41,L42,L47,L35
4. Page 31 use Audio port 2 , un-use port 1
5. Page 8 modify P04,P09,P07 and P059 to NTD4809NT4G , modify PQ40, PQ41, P05, P057, PQ10, PQ21 PQ50 and PQ53 to NTD4806NT4G
6. Page 19 add PR201, modify PQ13 to NTD4809NT4G , modify PQ11 and PQ12 to NTD4806NT4G
7. Page 20 modify PQ16 to NTD4809NT4G, modify PQ17 and PQ54 to NTD4806NT4G

5/11
1. Change PEC24 to 1000uF
2. Change part reference to solve silkscreen issue:
COM0 to SERIAL2
COM0 to SERIAL1
J1THERMD1 to THERM1
J1THERMD2 to THERM2
FAN_SYS to FAN_HDD
FRONT_PANEL to FRONTFANL
SATA0 to SATA_0
SATA1 to SATA_1
SATA2 to SATA_2
DIMM1 to DIMM_1
DIMM2 to DIMM_2
DIMM3 to DIMM_3
DIMM4 to DIMM_4

5/12
1.page38 Remove EC74
2.page38 Change EC75 from 470uf to 1000uf
3.page37 Add C57 for 24V per usb
4.page 23-25 Remove net Audio_CML_DETJ
Connect net WIRELESS_DETJ to ICH_AH21 instead of ICH_G8
5.page37 Add EC68 for 24V PWR USB
6.Remove TP108 and TP109
7.page 38 Add C3758, C130, and C3757 for com port 12V and 5V connection to GND

8. page 08 Add C1759
9. Change part reference
NIC_USB2 change to NIC_USB1
NIC_USB1 change to NIC_USB2
10.Change net name all LAN1 signal to LAN2 and all LAN2 signal to LAN1 (request from Dell EE request)

11.page 41 Add C254 0.1uF cap for SLOT6 3D3V_SB
12.page 43 Add C58, C65, C68 for PCI cross mod signals, FOR CLK_D00_33M C54 and POR Internal USB C56
13.page 35 Reserved R3091 and R3067 for PSU FAN TACH (Dell EE Request)
14. page 43 Add 8 dummy caps (request from Dell EMC feedback)
C71, C72, C85, C86, C87, C88, C89, C90
15.page24 update Board ID pop option
16. update DDR111 page information

5/15
1. page 20 PCI78 and PCI88 change from 0.22uF to 2.2nF.
2. page 19 change PQ83 from ZNT002 to 3904
3. page 8 change PR29 from 2K to 2.2Kohm

5/21
1. page 19 PFB12 , PFB14 , PFB27 change connection from 3D3V_SYS to 5V_SYS

5/22
1. page 19 change net name from 3D3V_SYS_IN to 5V_SYS_IN
2. page 4 updtie power delivery
3. page 1 add schematic approved table

5/27 refer deviation to update
1. Page 23 R278 dummy
2. Page 32 GR27 8.2K --> 30K
3. Page 40 OR22 8.2K --> 30K
4. Page 19 PR194 8.2K --> 5.1K/-1% , PC100 3.3m -->1nF , PR184 dummy
5. Page 7 mount R58,R587,R556 and dummy R48,R46,R28
6. Page 10 dummy R231 , R299
7. Page 27 mount LR14,LR15 and dummy LR1,LR2
8. Page 20 PR408 33K(dummy) --> 150K , PR321 0(dummy) --> 3.24K , PR322 dummy

01/30: Add ERP 0.5W Solution
1. Page 35 B1X PWR Connector的第8Pin由5V_SB_SYS變更為ATX_V5VB, 連接到ERP 0.5W Solution的輸入端, 其他地方的沒有變化
2. Page 40 FRONTPANEL的第__Pin增加offpage Netname, 連接到ERP0.5W Solution的相應Pin,R436左端Netname由原来的PWR_BTNJ_D變更為PWRBTN_ERP#, 是由ERP0.5W Solution拉過來的開機信號,Change PWR_SNH to PWR_BTNJ_D
3. Page 40 Delete R3008
4. Add Page 43--ERP0.5W Solution, 其他頁次順延
5. Page 24 Board ID變更, Dummy R2334, Add R3334
6. Page 35:Change pull up power for P8_ONJ from 5V_SB_SYS to ATX_V5VB,增加一個5V_SB_SYS的decoupling電容ERP_C5,增加一組AUX_PWR線路(ERP_R12和ERP_AUX_PWR), 原来的AUX_PWR線路中的電阻和發光二級管Dummy掉, 預留位置

X00 TO X00 change list

7/13
Page 13 change R528 form 475 to 499
Page 32 change net name from THERMDA_PUS to THERMDA_PUSU
swap pin 1 , 2 of THERM1
Page 43 change H10 , H18 footprint from mh6_35MM to mh40x80_8_dell
Page 9 R682 use 576 ohm and R680 use 1.3 Kohm

Power
Page 4 Change 1D5V_ICH from Linear to Single Phase Switch Solution and change input source to 3D3V_SYS
Page 8 Change PC23 from 15nF to 6.8nF
Change PEC45 from 820uF to dummy

Page19
1. RemovePR183 PR184 PR217 PC102 PC103 PC190 PC191 PEC26 PRN1 PRN2 PQ20
2. Add PFB15 Bead at 1D5V_ICH input side
3. Add 22uF for PC98 PC99 PC101
4. Add 0.1uF for PC108 PC110 PC111 PC112
5. Add 1nF for PC109
6. Add 33pF for PC83(dummy)
7. Add 10kohm for PR721 PR722 PR723
8. Add 1kohm for PR724
9. Add 330kohm for PR104
10. Add 24.3kohm for PR105
11. Add 150kohm for PR106
12. Add 133kohm for PR107
13. Add 0 ohm for PR132
14. Add WMGT3906LT1Q for PQ104
15. Add WMGT3906LT1Q for PQ105
16. Add RTW015AQM for PUS
17. Add 1uH for PU10
18. Change PR215 from 1.3kohm to 13kohm
19. Change PR208 from 1.21kohm to 12.1kohm
20. Change PR117 from dummy to 1kohm
21. Change PR354 from dummy to 4.7kohm
22. Change PQ137 from dummy to WMD5551
23. Change PR117 pull high level from 1D5V_ICH to 1D1V_MCO_PG

Page20
1. Change PR315 from 0 ohm to dummy
2. Change PR316 from dummy to 0 ohm
3. Change PR296 from 1.82kohm to 1.87kohm
4. Change PR321 from 3.24kohm to dummy
5. Change PC97 from 10uF to dummy
6. Add 0 ohm for PR316 to contact ATXPWRKD with PU12 Pin4

7/14
Page 27 add L1J3 (Atmel EEPROM) for second source
Page 35 change R477 from 10K to 8.2K ohm
Page 16,17 update DIMM slots to gold plating 20 u"

7/16
Page 37 change component name form LPC-DEBU01 to LPC-DEBU0
Page 43 change H18 and H10 footprint name from MH40X80_8_DRL1_216
Page 27 mount LRL1 , LR2 and dummy LRL4 , LR15

7/17
Page 38 change serial 1/2 footprint name from dsusb2m9h319 to dsusb2m9_1h319
pin swap
CN6.5 NCTSA
CN6.3 MDSRA
CN6.1 MDTSA
CN7.7 MDTSA
CN7.5 NSIHA
CN7.3 NSCOTTA

7/20
Page 38 update J2 , J3 , J4 , J5 jumper table

7/21
Page 38 update pare reference J2 --> J4 , J4 --> J2 , J5 --> J1

7/25
Page 13 add PWR
Page 20 change PU21 from TP85422310 ES SM090703SD
Page 1 remove the text "waiting for Dell to confirm support to 1333 or 1066"
Page 3 update logic grouping (COM0 and DIMM) are channel 0, J1702 and DIMM are channel B.
Page 35 add SC15 47nF
Page 36 all the coding/net name of FAN_SYS change to FAN_HDD
Add R447,R448,R573,R572,R571,R489
and Dummy R261,R239,R312,R311,R310,R279 to connect SMbus to PCIe and PCI slots

X01 TO A00 change list
11/3 change audio codec to version VB3
11/12 Stuff PEC25 470uF for 3D3V_SB to reduce voltage drop from S5 to S0 or G3 to S0
11/24 Page23 Change R548 and R549 from 2.7K to 8.2K to reduce SMBUS voltage Drop during Power up and Power down.